

Compal Confidential

DH53F MB Schematic Document

LA-F991P

Rev : 1.C

2018.02.13

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/07/20	Deciphered Date	2018/07/20	Title	Cover Sheet
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				Sheet	1 of 73
				Rev	1.A

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{BI} D min	V _{BI} D typ	V _{BI} D max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VS)	N17E-G1 (VGA)	0x9E		
	EC			
	CC controller 179F			
	TMS			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 Level	Description	BOM Structure
431AB2BOL05~08		
431AB2BOL53_54		
431AB1BOL67		
X4EAB2BO001		
X4EAB2BO051		
X76730BOL56	ALT. GROUP PARTS N17E6G SAM 256M32 DH7VF	
X76730BOL57	ALT. GROUP PARTS N17E6G HYN 256M32 DH7VF	
X76730BOL58	ALT. GROUP PARTS N17E6G MIC 256M32 DH7VF	

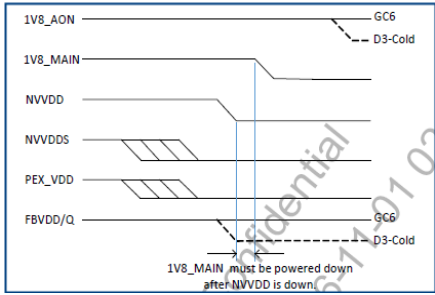
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

Item	BOM Structure
Unpop	@
Connector	CONN@
UMA only	UMA@
CMC	CMC@
dGPU	VGA@
DIS only	DIS@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
28P keyboard connector	28P@
32P keyboard connector	32P@
Finger Print	FP@
Finger Print for ESD	FPESD@
PBA	PBA@
Thermal sensor	TMS@
LAN LDO mode	LDO@
LAN Switch mode	SWR@
G-Sensor	GSEN@
EMI requirement	EMI@
EMI require reserve	@EMI@
ESD requirement	ESD@
EMI require reserve	@ESD@
CNVi	CNVi@
UART debug	UART@
Codec ALC255	255@
Codec ALC256	256@
Codec ALC256 for ESD	256ESD@
Codec ALC256 for EMI	256EMI@
G-PAK for GPU sequence	GPK@
DIS for GPU sequence	NGPK@
W/ SATA re-driver	SATARD@
W/O SATA re-driver	NORD@
PCH	PCH@
CPU	i5@/i7@

Power Plane	Description	S0	S3	S4	S5
+RTCVC	RTC Battery Power	ON	ON	ON	ON
+19V VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW PCH PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW SPI	+3VALW PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS VCCSTG	+1.05VALW PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA CORE	Core voltage for VGA (merge core & core s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID	PCB Revision
0	0.1 / 28P
1	0.2 / 28P
2	1.0 / 28P
3	1.C / 28P
10	0.1 / 32P
11	0.2 / 32P
12	1.0 / 32P
13	1.C / 32P



DH53F_EVT Power Sequence

BIOS : 0.05

AC mode

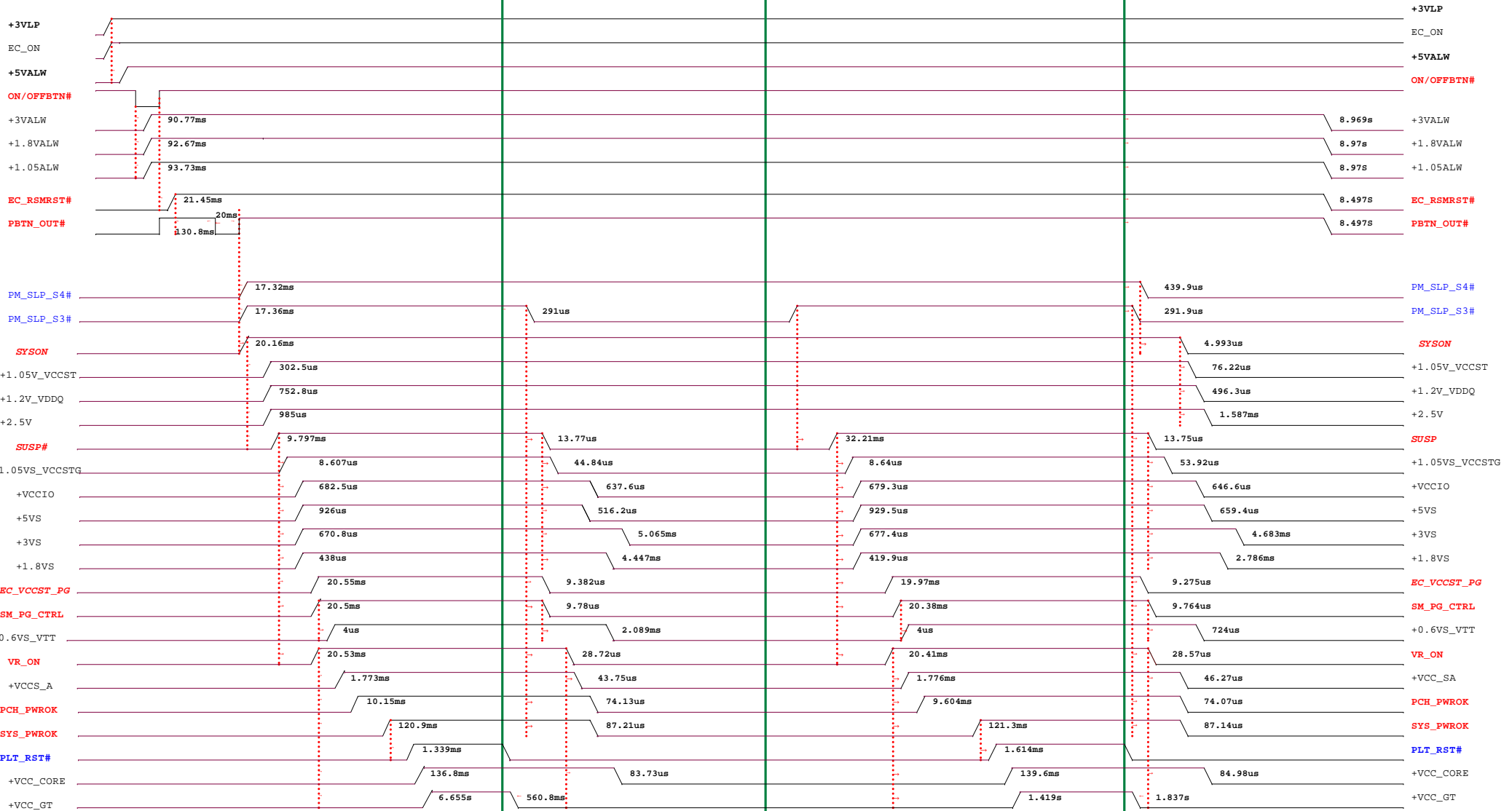
Power On

S3

S3 Resume

Power Off

Plug in



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PCB@ DAZ29000103
PCB DH53F LA-F991P LS-F992P/E921P

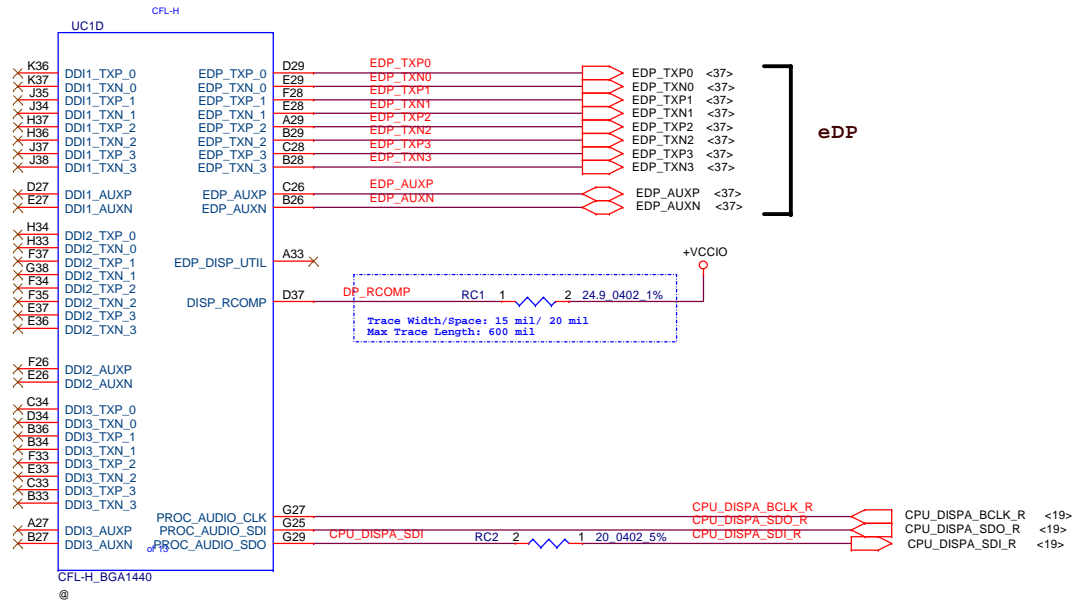
Coffee Lake-H CPU SKU



CFL-H_BGA1440
S IC CL8068403373522 SR3Z0 U0 2.3G ABO1
SA0000BPJ40
5@



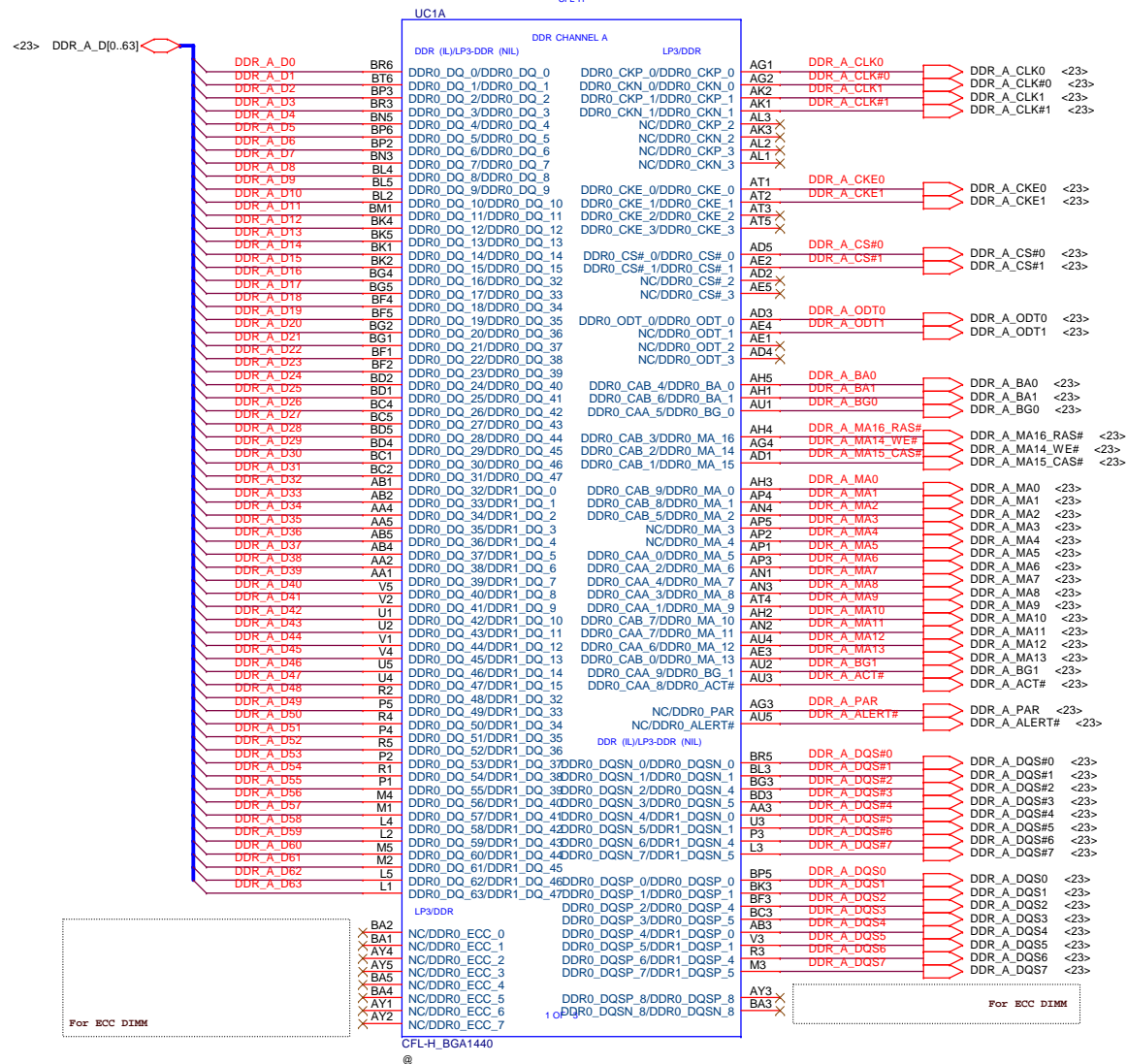
CFL-H_BGA1440
S IC CL8068403359524 SR3YY U0 2.2G ABO1
SA0000BPZ40
17@



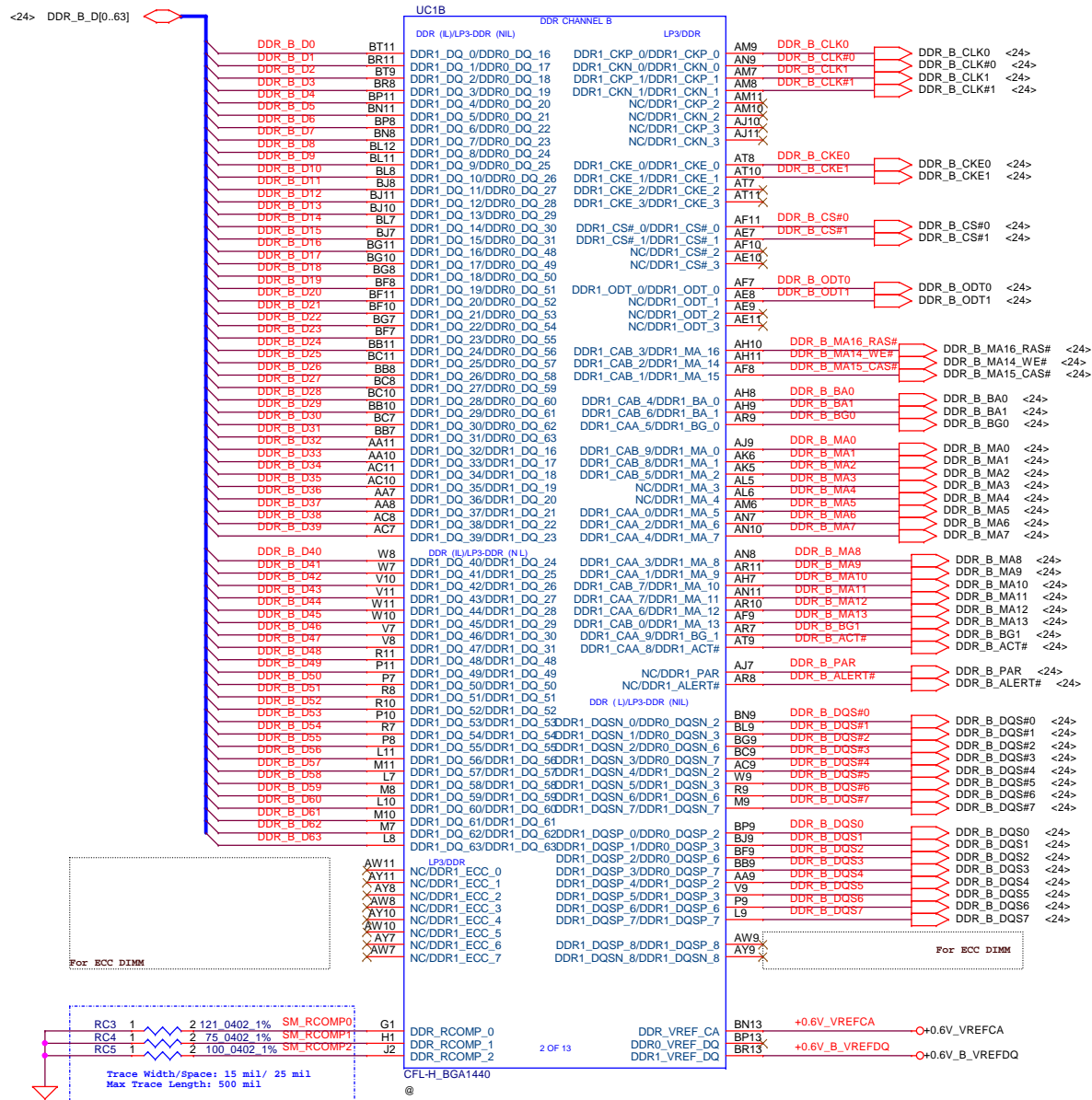
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Issued Date	2017/07/20	Deciphered Date	2018/07/20	Title	CFL-H(1/8)DDI/eDP
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CHANNEL-A

Interleaved Memory

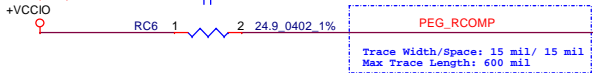
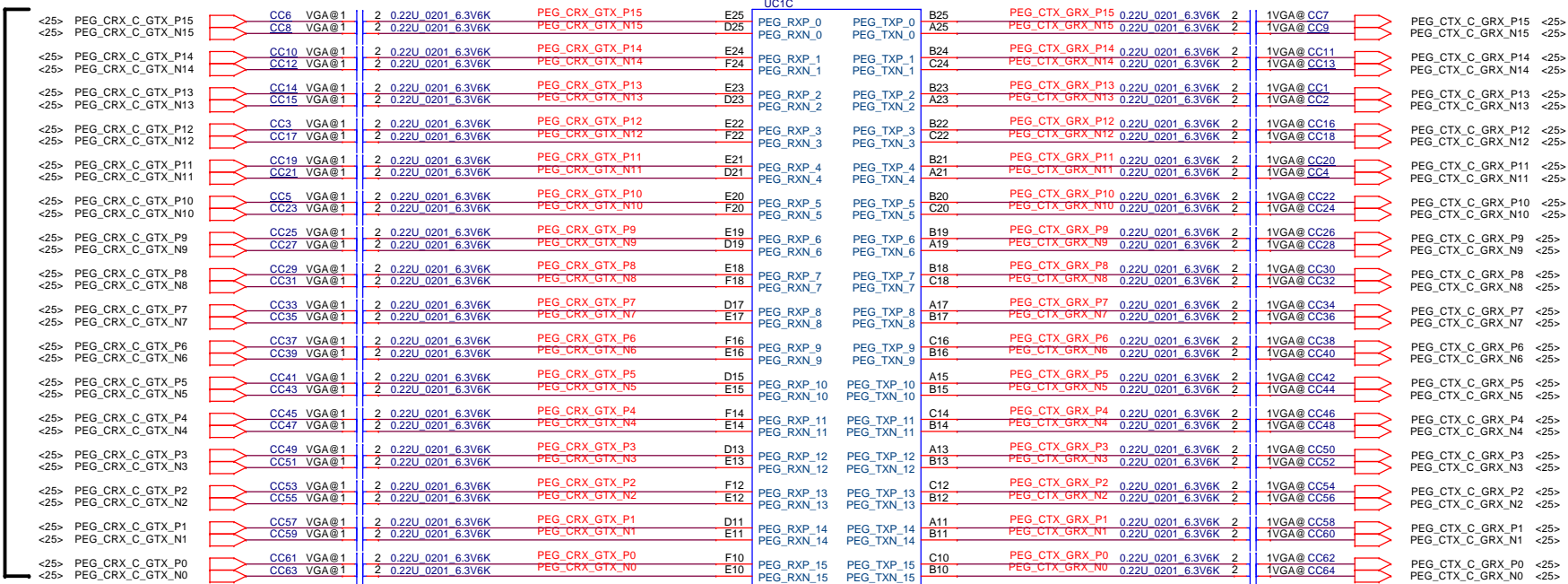


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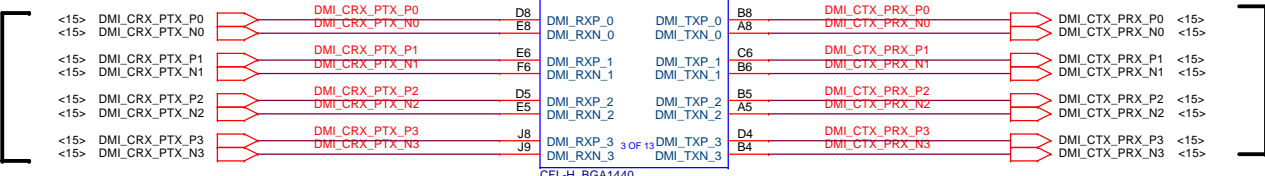
To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed



To PCH

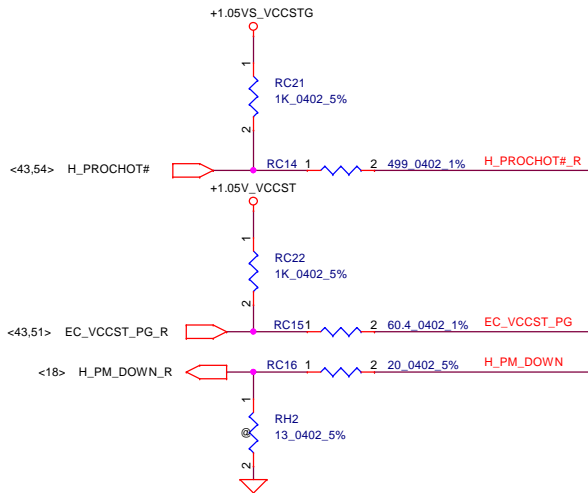
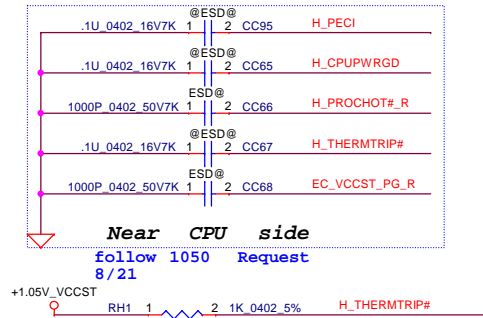
To PCH



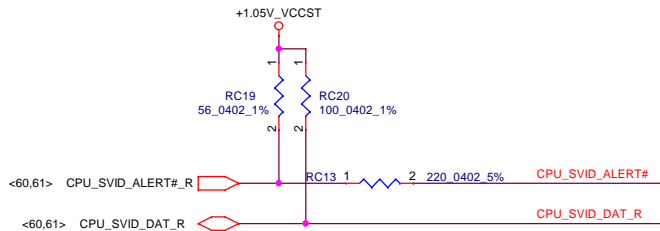
CFL-H_BGA1440

571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

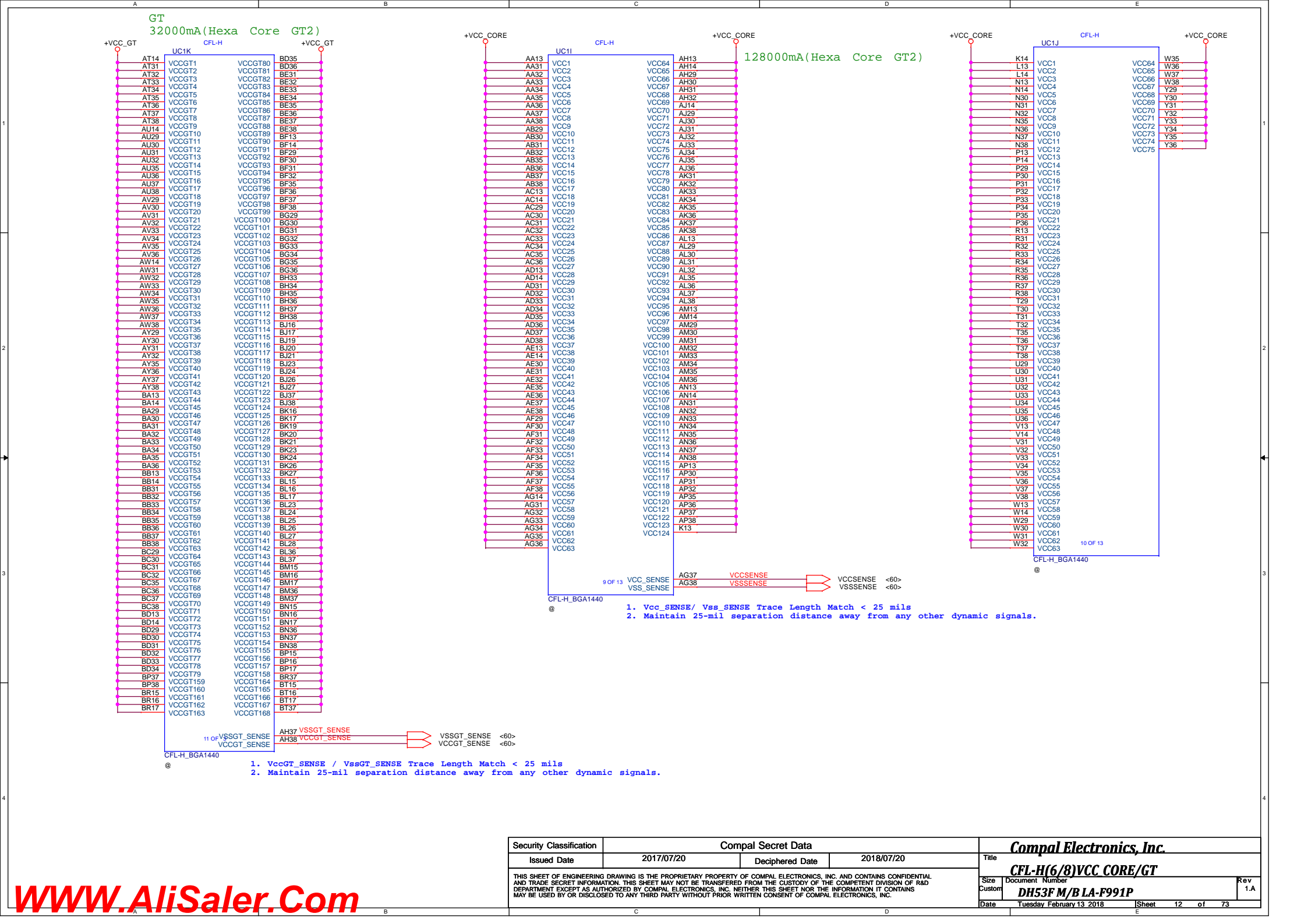
PROC_SELECT#
should be unconnected on CFL processor
EDS1.2 8/21

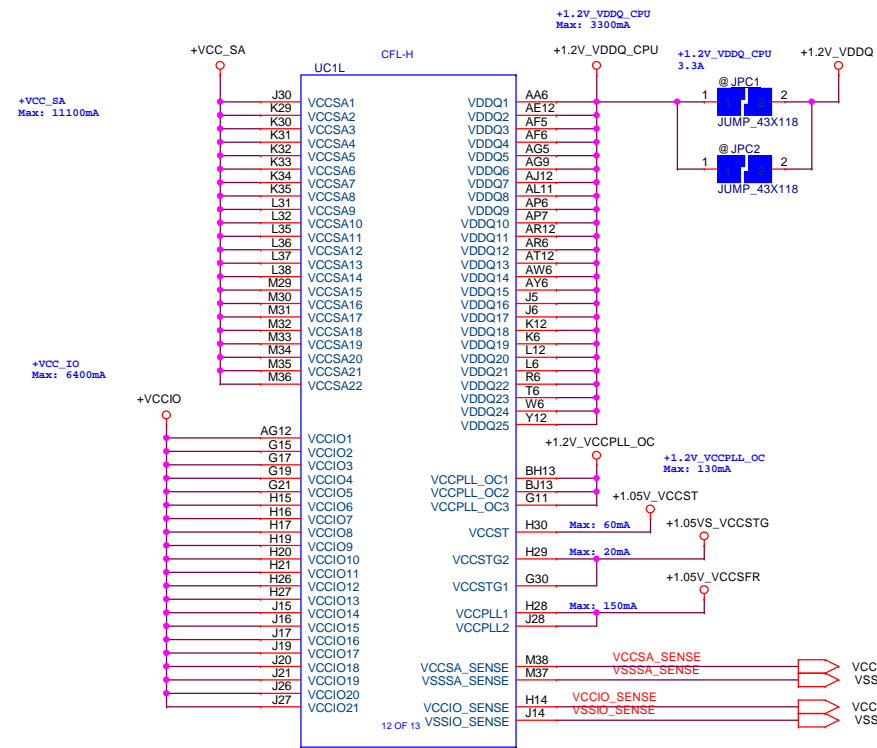


SVID

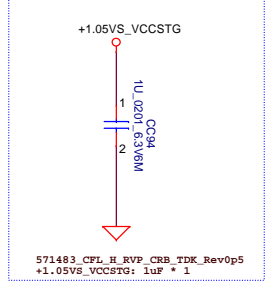
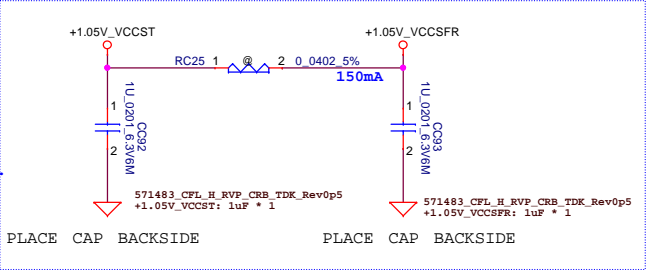
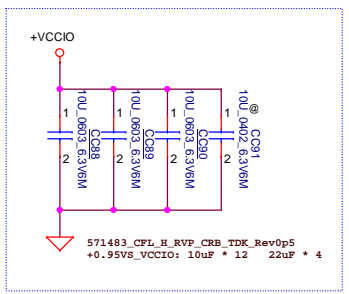
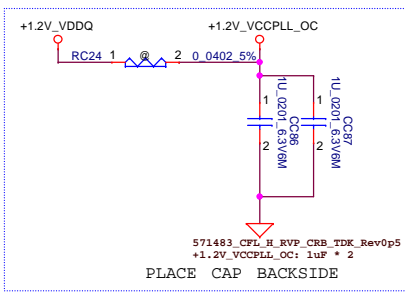
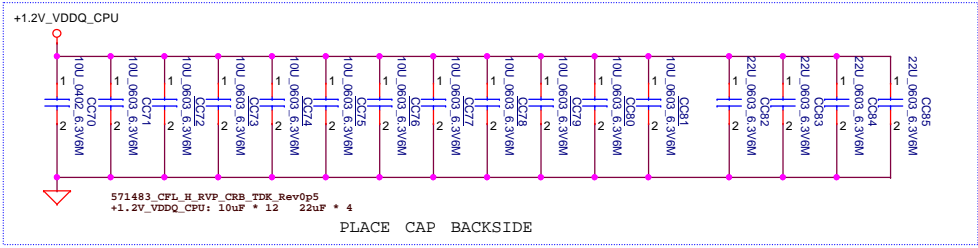


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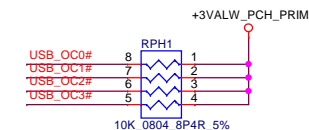




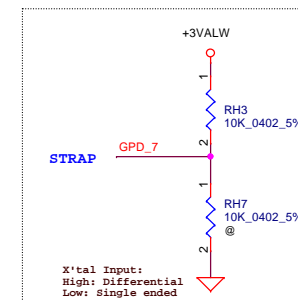
1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



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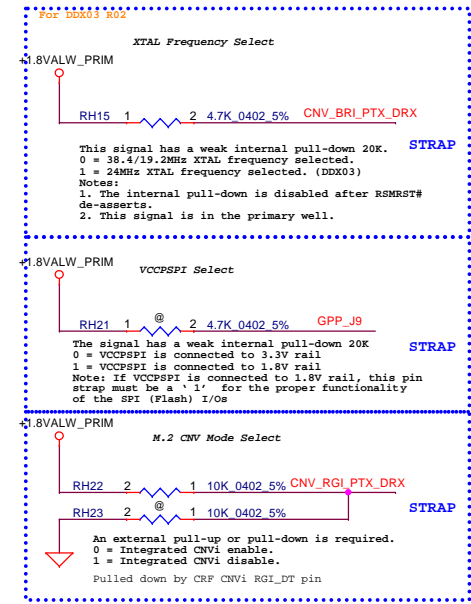
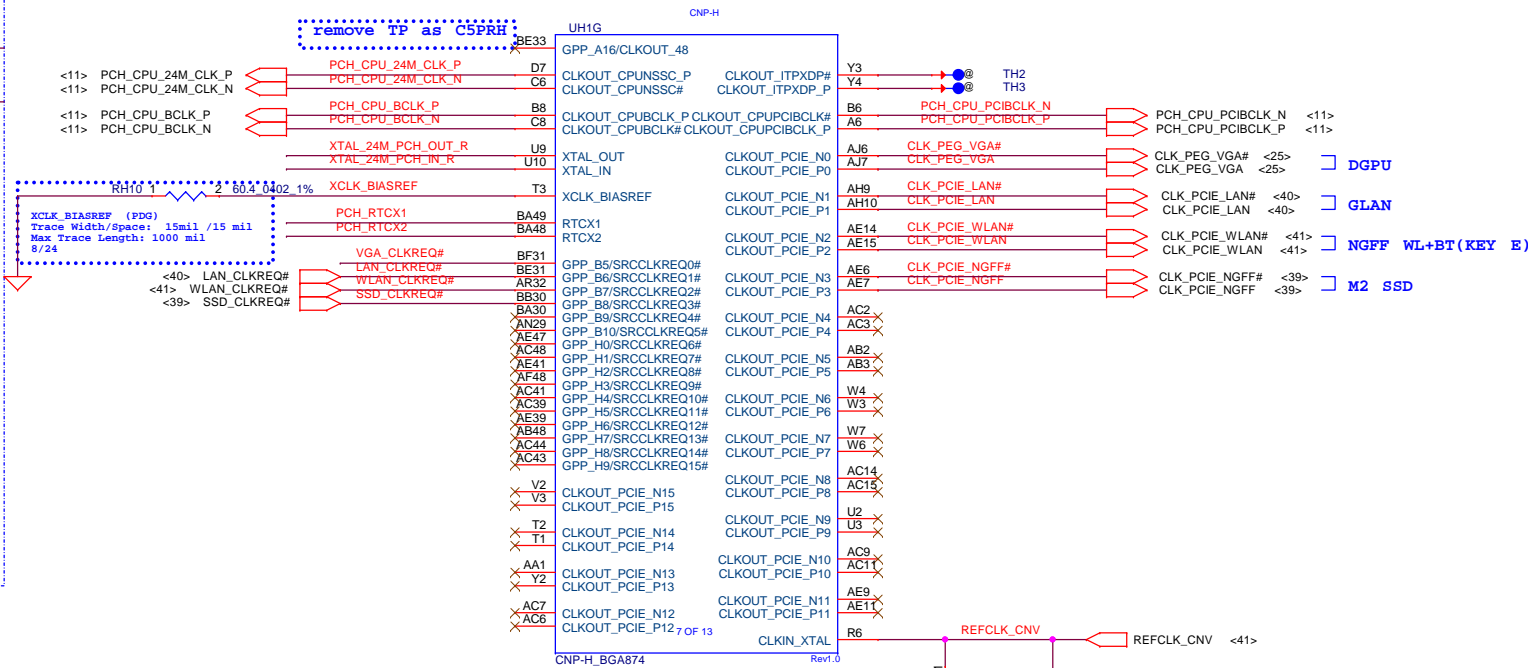
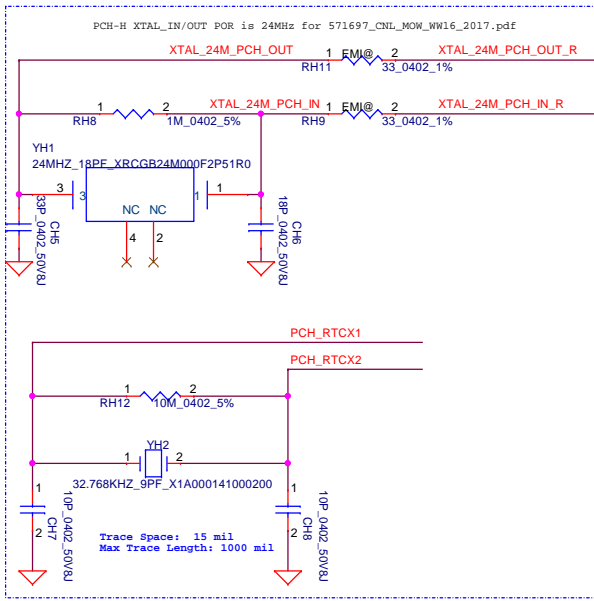
FOR CNVI follow 571906_CNL_PCH_TA_WW11.pdf



The 30 HSIO lanes on M100-H supports the following configurations:

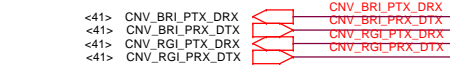
1. Up to 24 PCIe* Lanes
 - A maximum of 16 PCIe* Ports (or devices) can be enabled
 - When a GBE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
 Max PCIe* Ports (or devices) = 16 - GBE #1 (0 or 1)
 Max PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
 - A maximum of 6 SATA Ports (or devices) can be enabled
 - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 6 or 18
 - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
 - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GBE Lanes
 - A maximum of 1 GBE Port (or device) can be enabled
5. Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
 - x2 and x4 PCIe* NVMe SSD
 - x2 Intel® Optane® Memory Device
 - See the "PCI Express* (PCIe*)" chapter for the PCI PCIe* Controllers, configurations, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support
6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA*, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Configuration discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

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remove SD signal from PCH

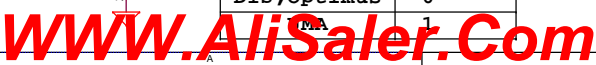
remove CPU_C10_GATE#

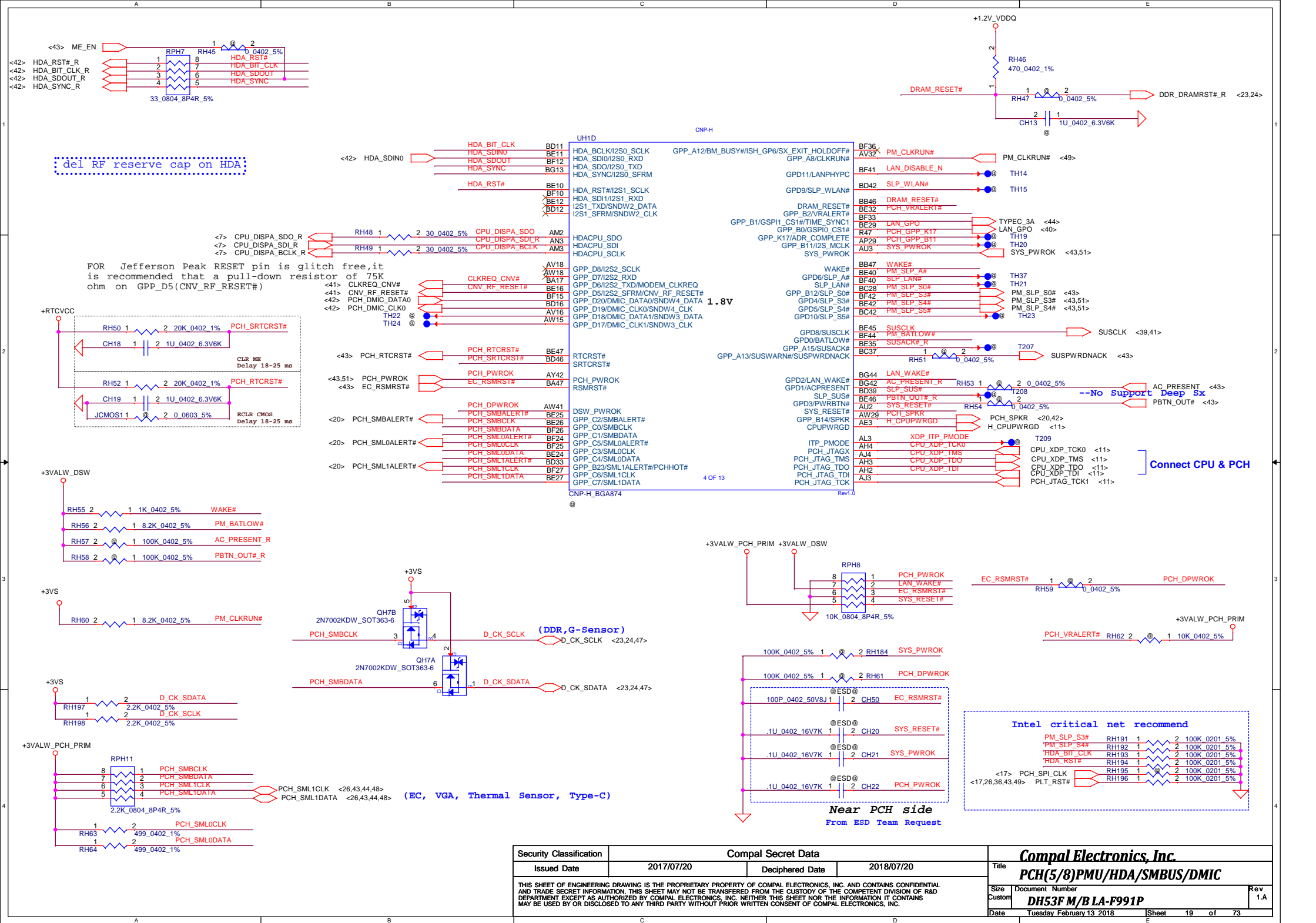


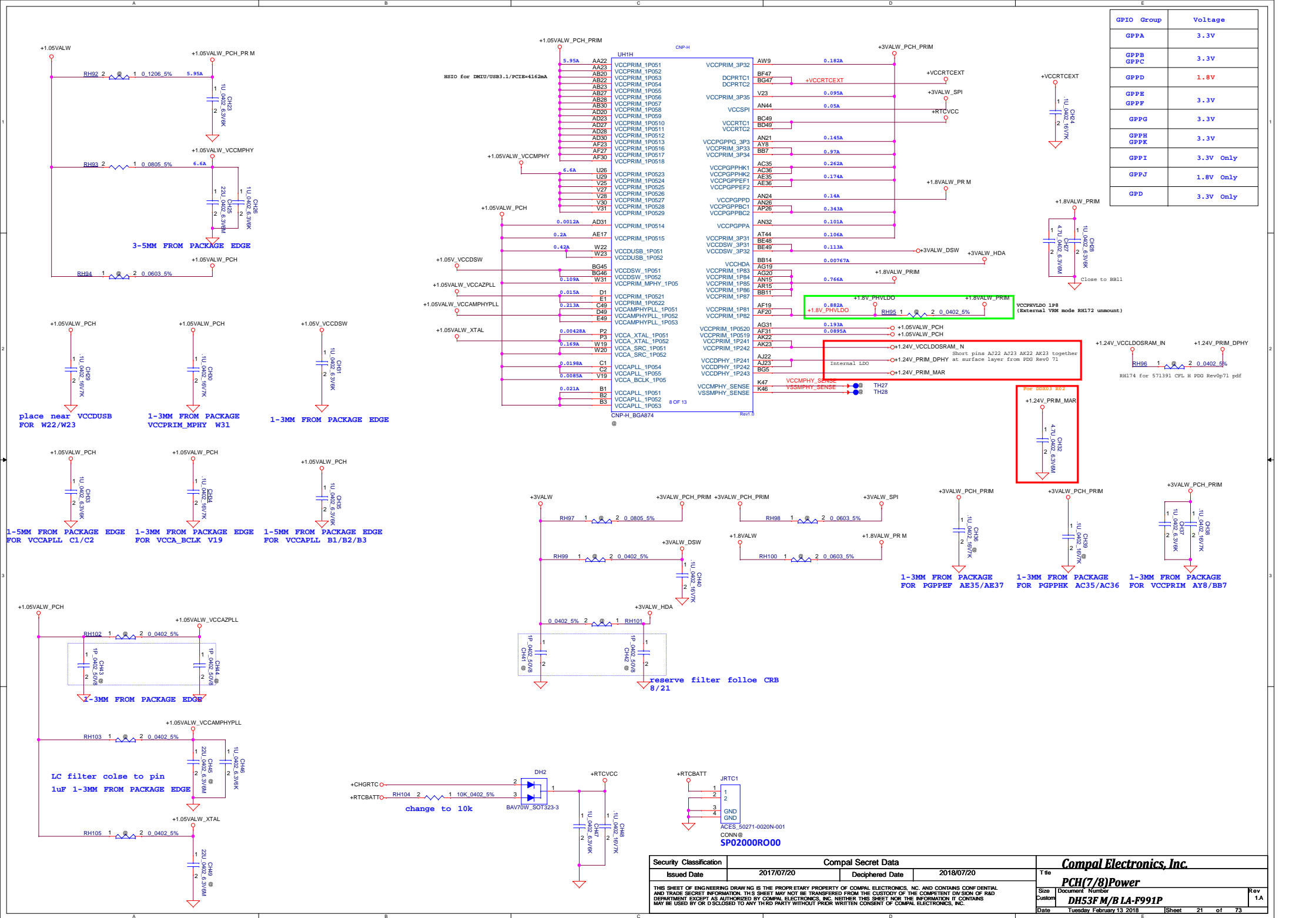
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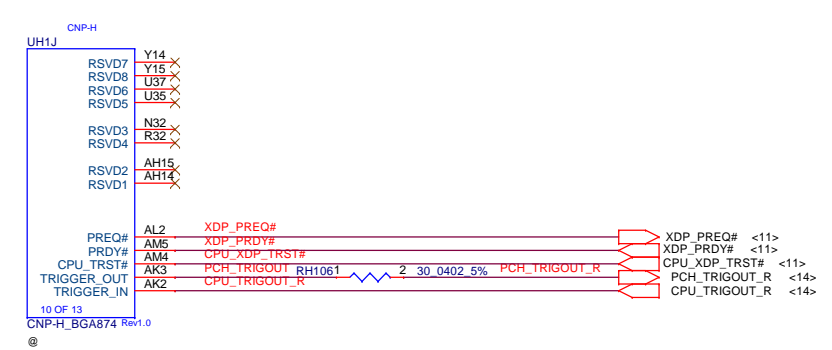
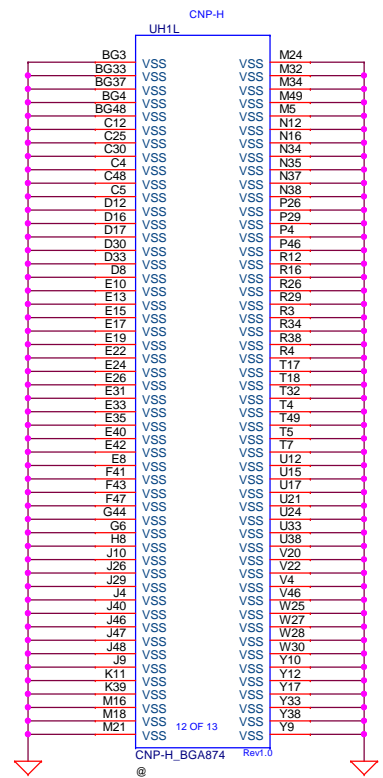
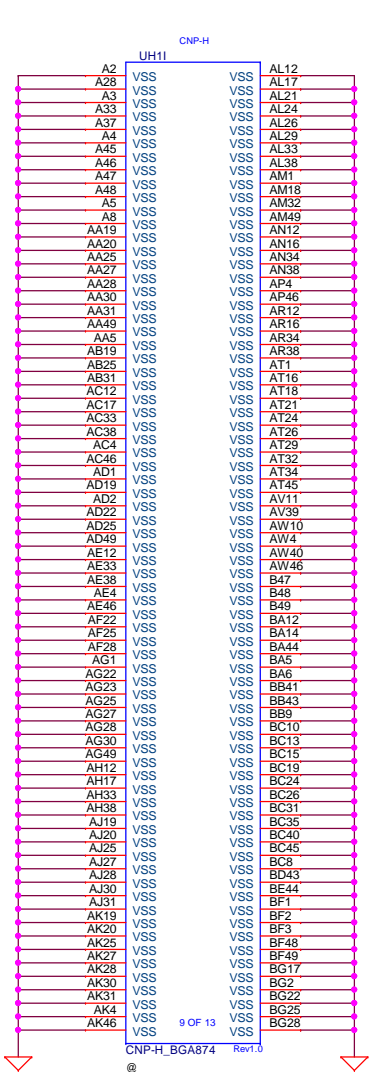
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

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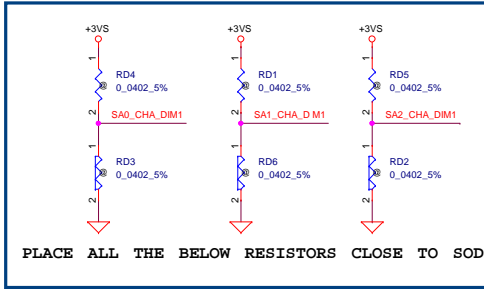
CHANNEL-A

BOT

REVERSE TYPE (4 mm)

Interleaved Memory

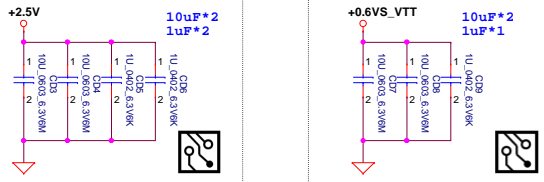
TOP: JDIMM1 CONN Non-ECC DIMM



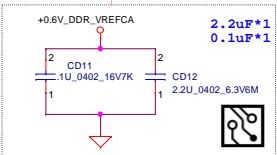
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

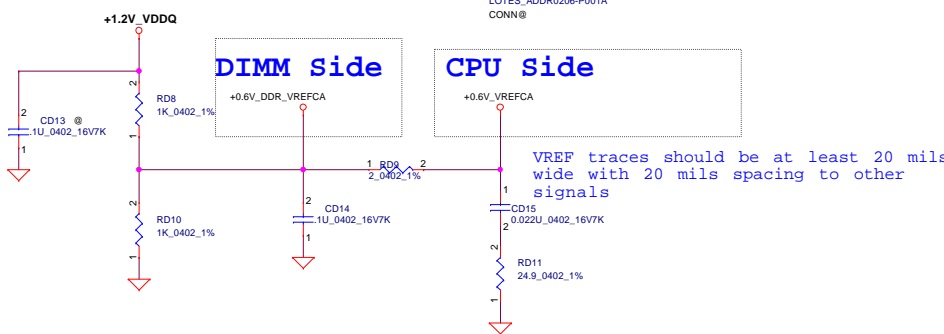
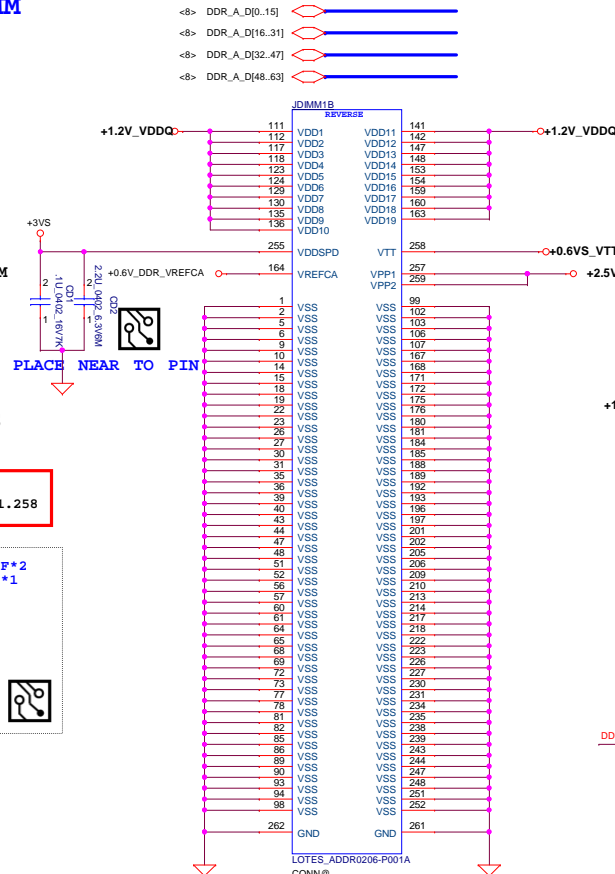
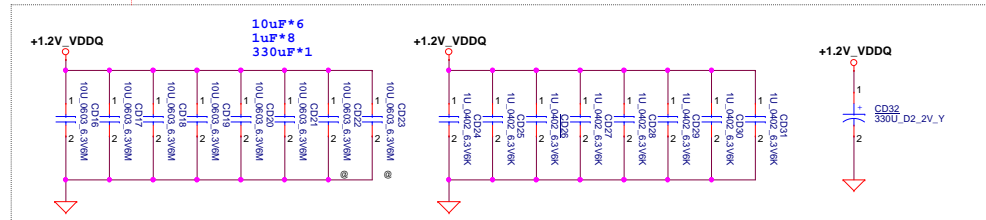
Layout Note:
Place near JDIMM1.258



Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1



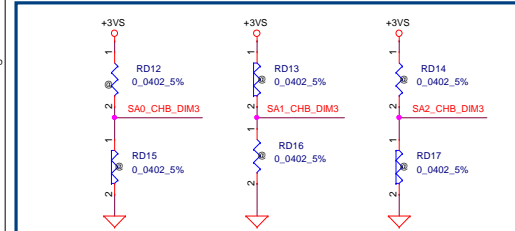
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2017/07/20		Deciphered Date		2018/07/20		Title			
								DDRIV_CHA: DIMM0			
								Size			
								Document Number			
								DH53F M/B LA-F991P			
								Date			
								Tuesday February 13 2018			
								Sheet			
								23 of 73			

CHANNEL-B

BOT REVERSE TYPE (8 mm)

Interleaved Memory

TOP: JDIMM3 CONN Non-ECC DIMM

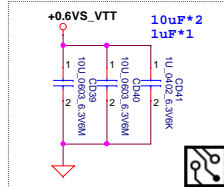
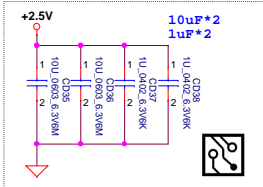


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

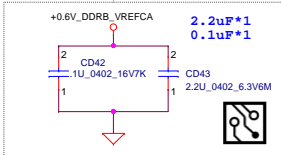
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM3.257,259

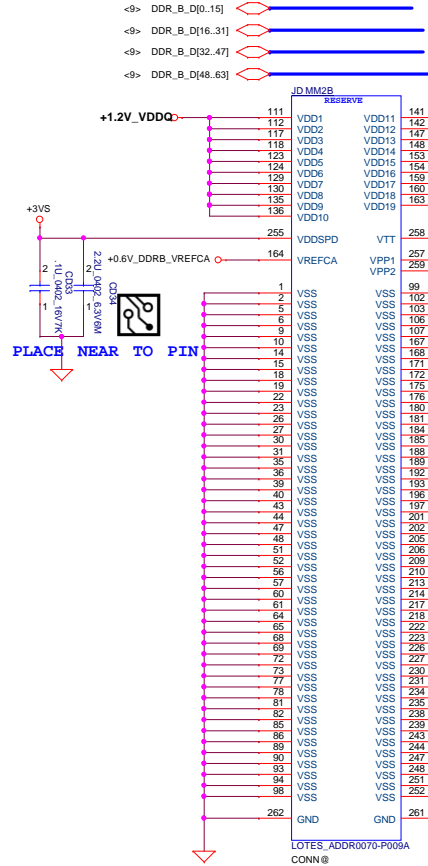
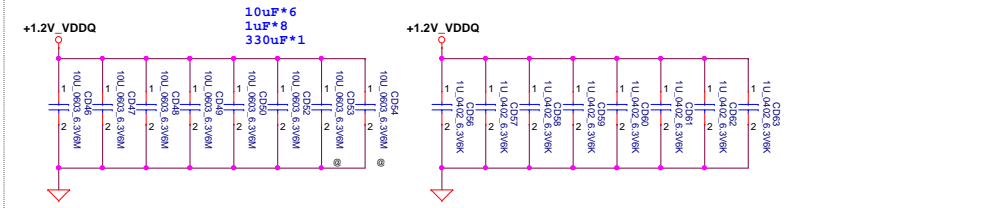
Layout Note:
Place near JDIMM3.258



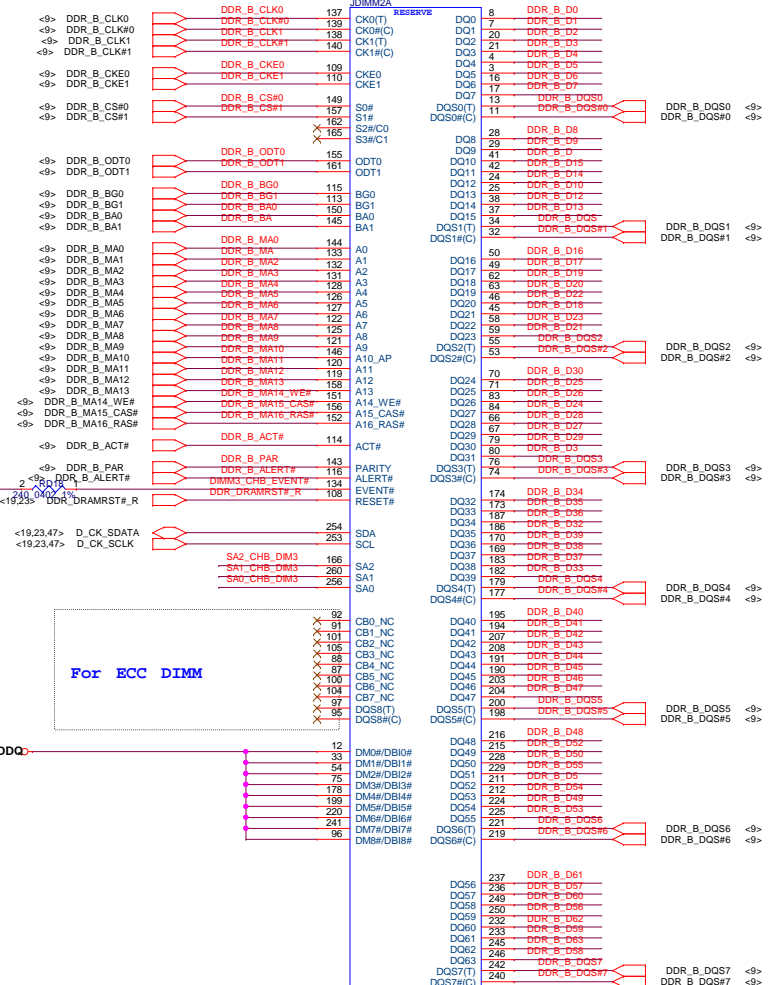
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



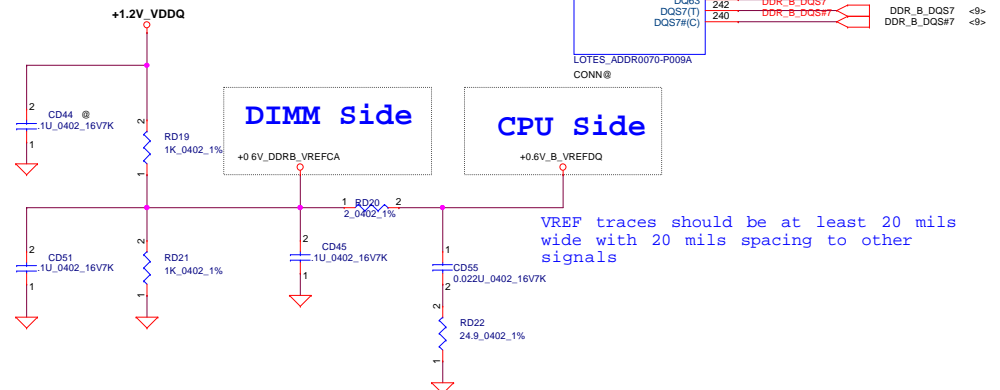
Layout Note:
Place near JDIMM3



PLACE NEAR TO PIN

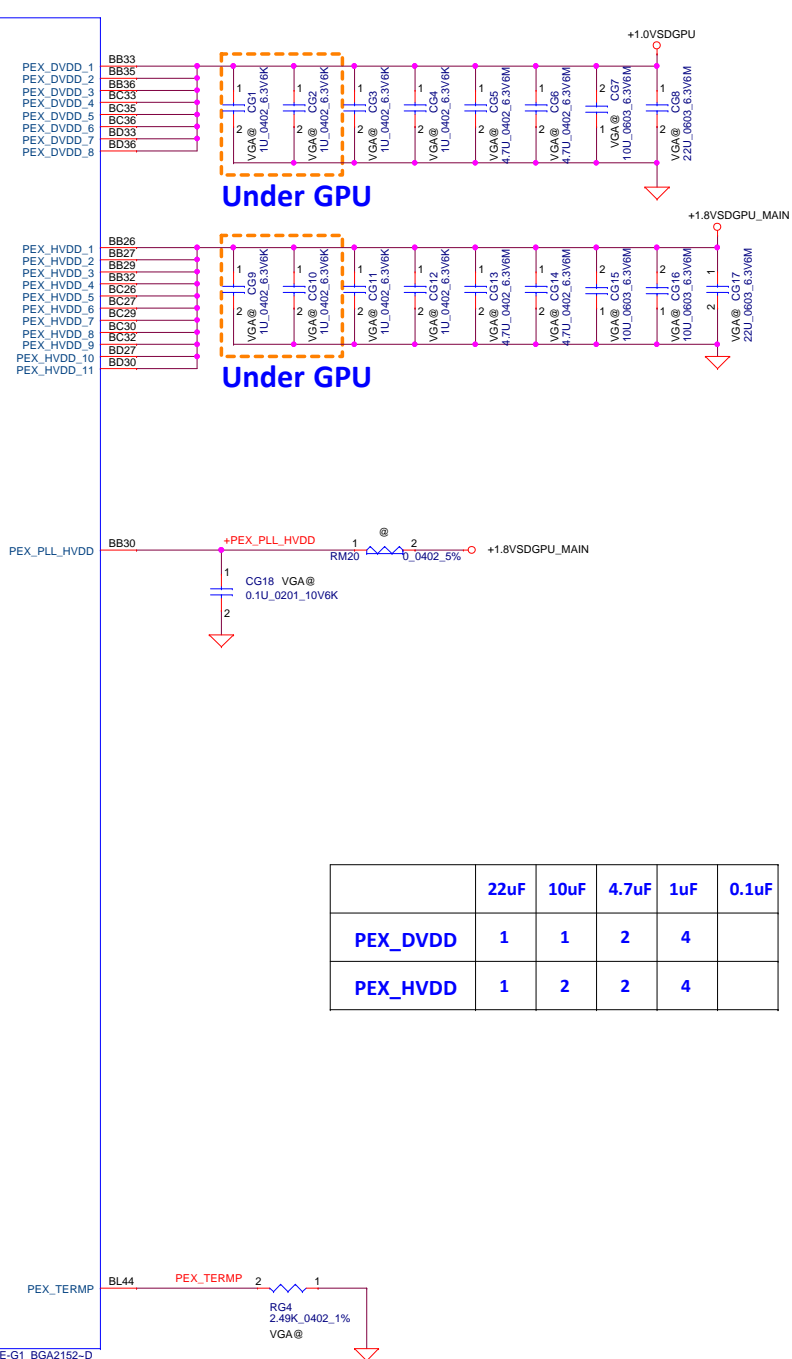
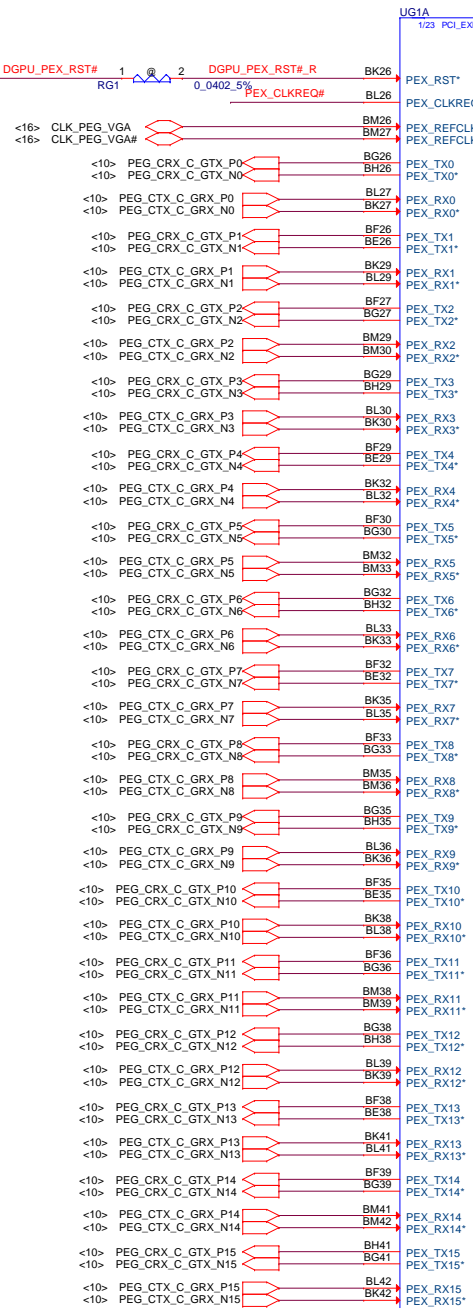
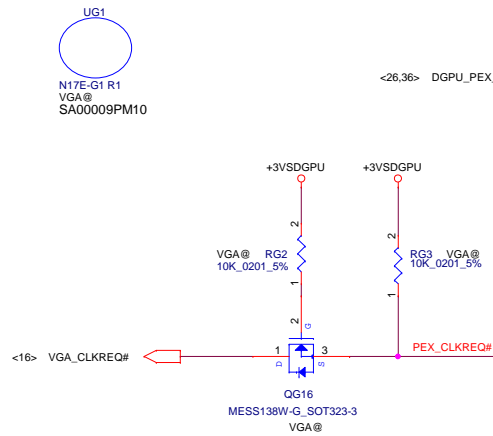


For ECC DIMM



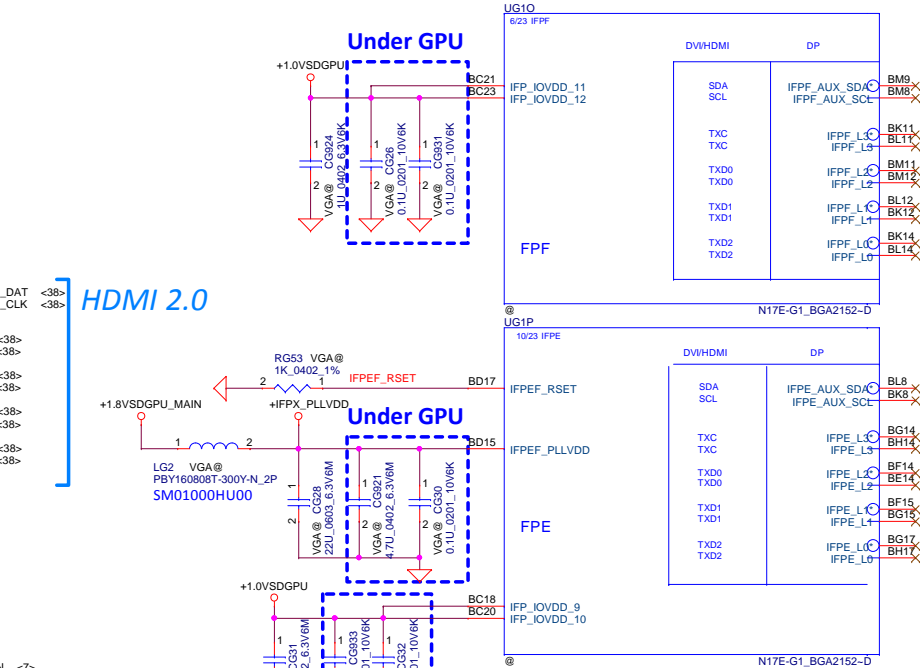
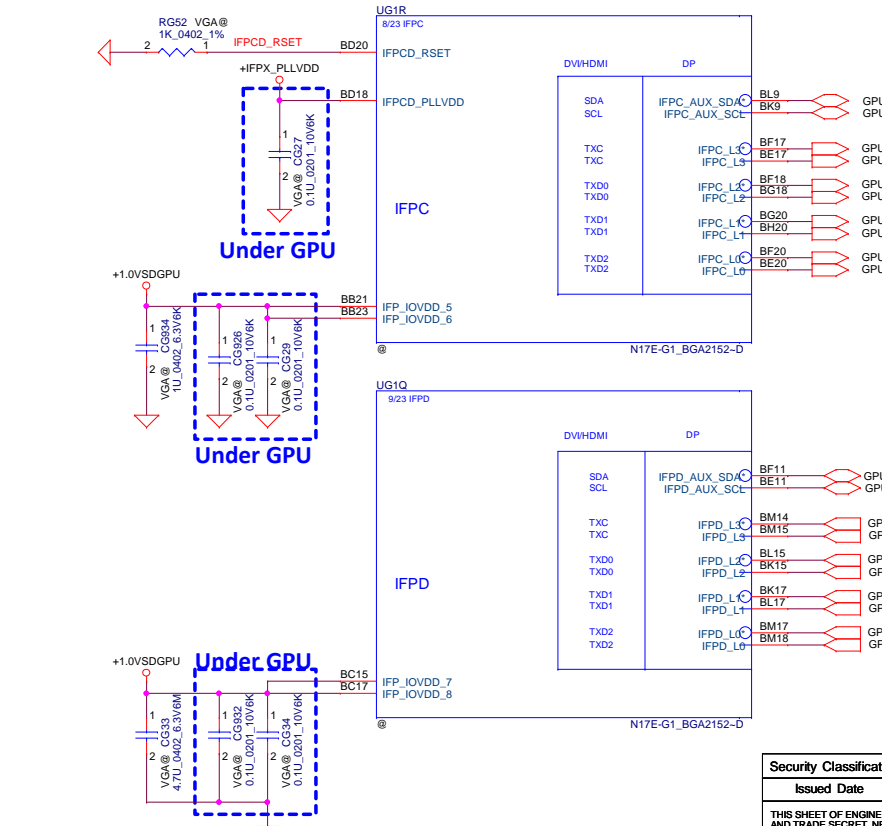
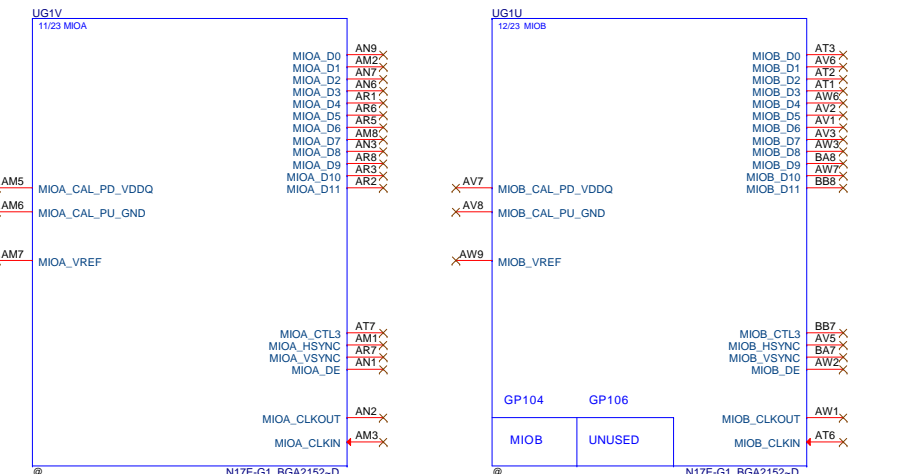
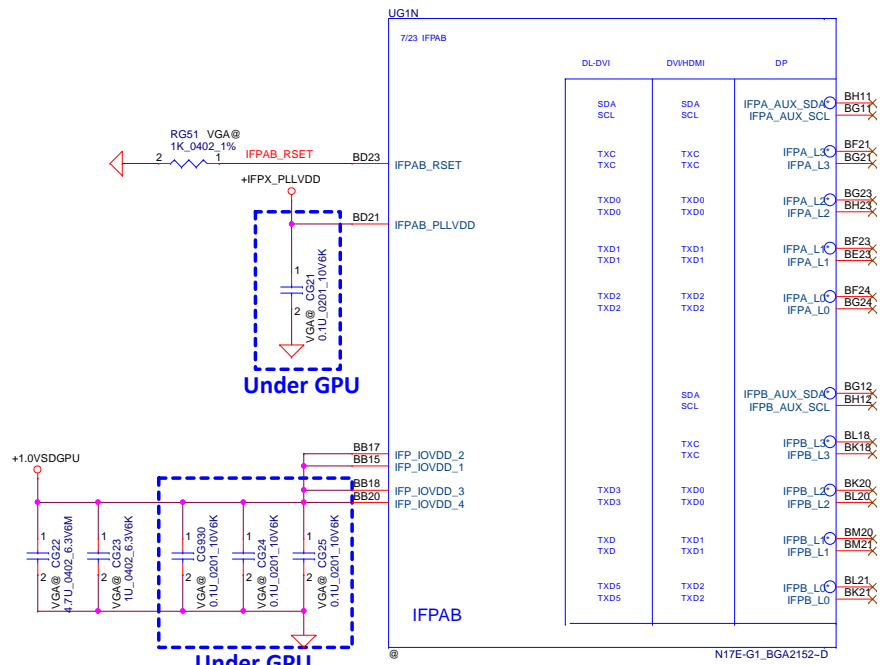
VREF traces should be at least 20 mils
wide with 20 mils spacing to other
signals

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	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

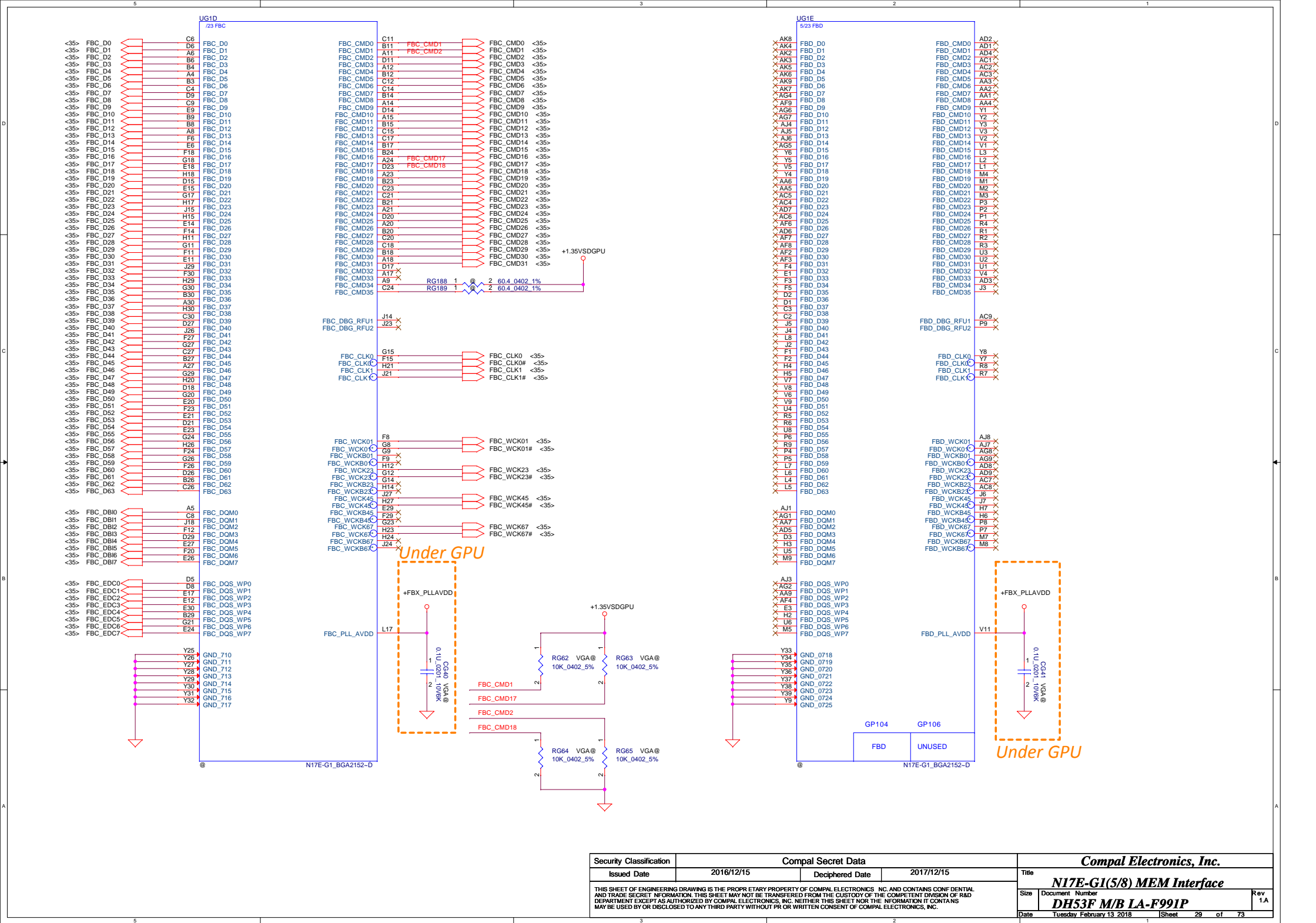
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/12/15	Deciphered Date	2017/12/15	Title	N17E-G1(1/8) PCIE
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				Model	DH53F M/B LA-F991P



HDMI 2.0

	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			3	3	12
IFPx_PLLVDD	1		1		3





Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2016/12/15		Deciphered Date		2017/12/15		Title			
								N17E-G1(5/8) MEM Interface			
								Size Document Number			
								DH53F M/B LA-F991P			
								Rev 1.A			
								Date Tuesday, February 13, 2018			
								Sheet 29 of 73			

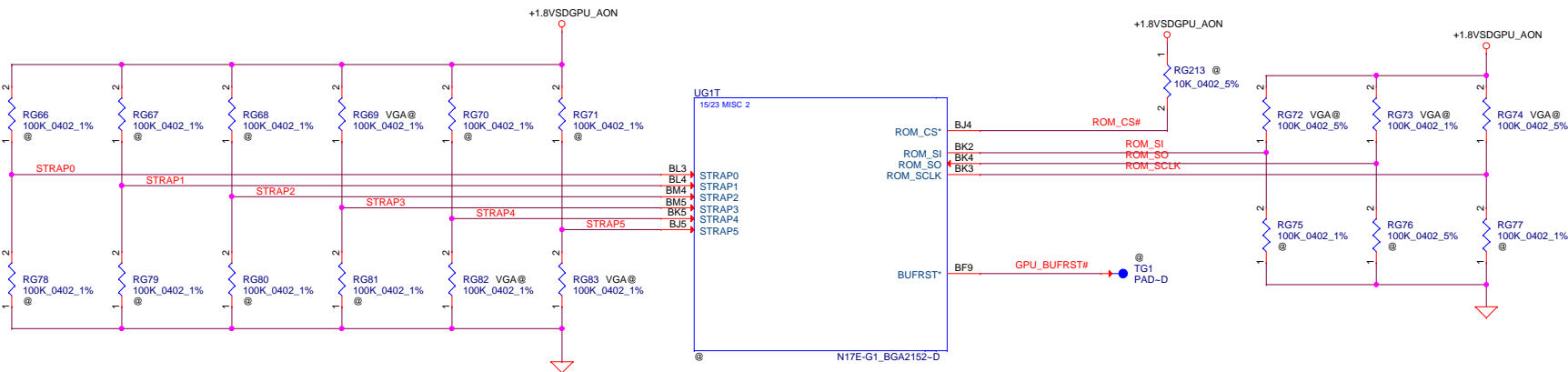


Table 2. N17E-G1 GDDR5 Recommended Memories

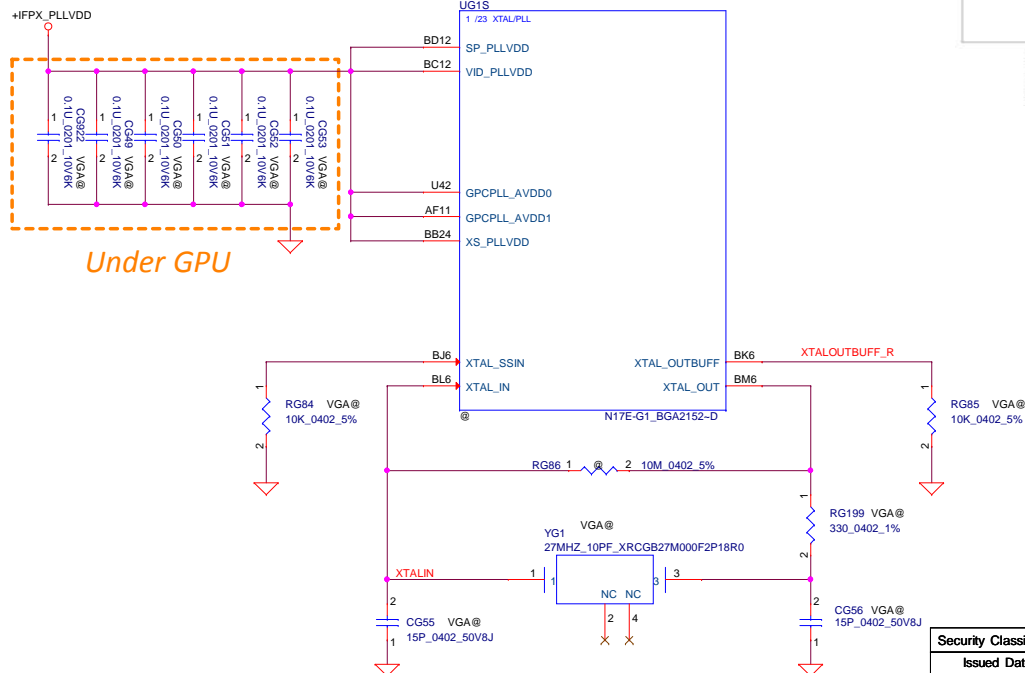
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V ²	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V ²	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V ²	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready
4 Gb	128Mx32	1.35V and 1.55V ²	Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	Full	Post production ready
		1.35V and 1.55V ²	Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	Full	Post production ready

Notes:

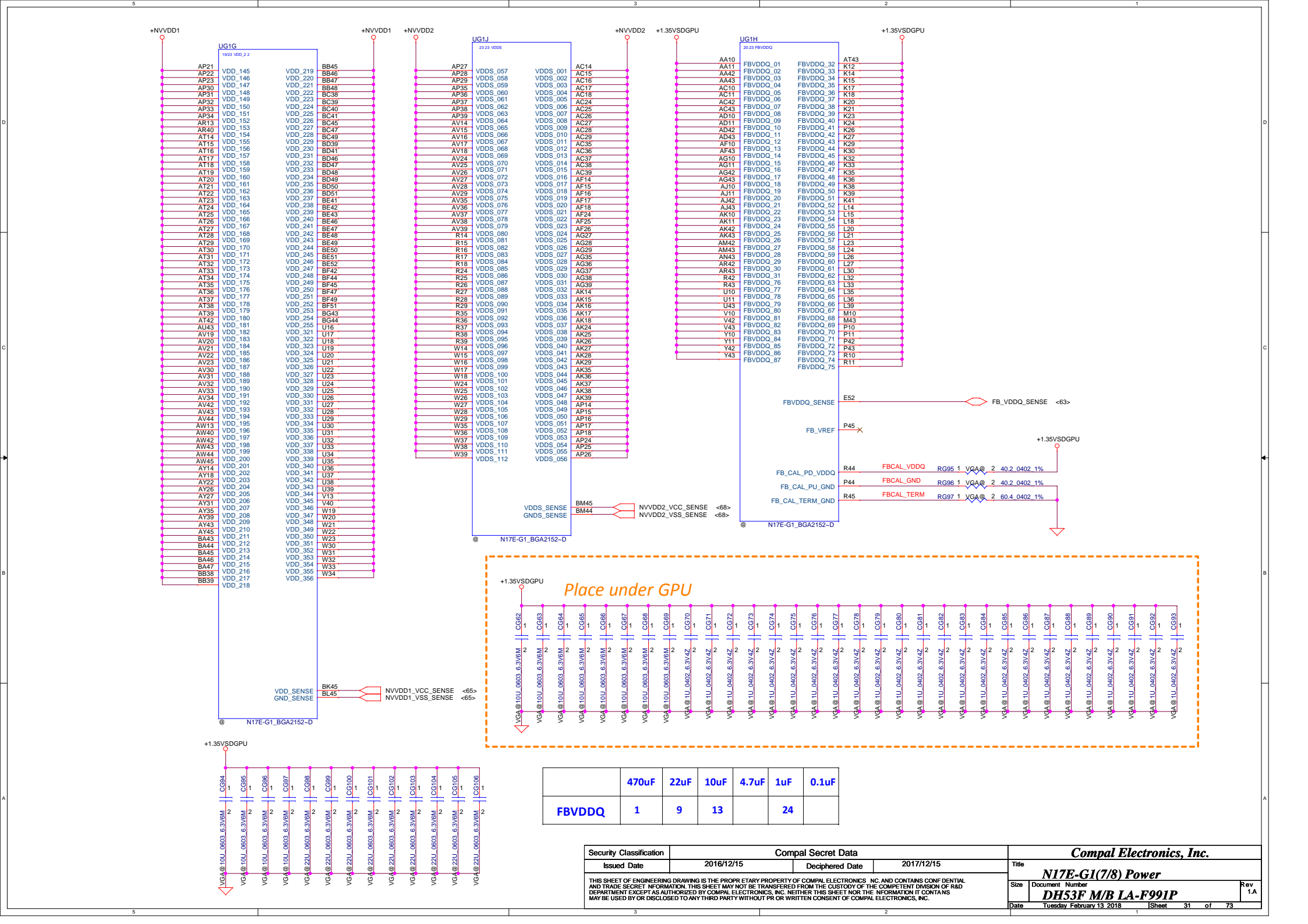
- For N17E-G1, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
- N17E-G1 runs WCLK up to 3000 MHz with FBVDD = 1.35V. DV5 is required to run WCLK > 3000 MHz.

Table 5.3 RAMCFG

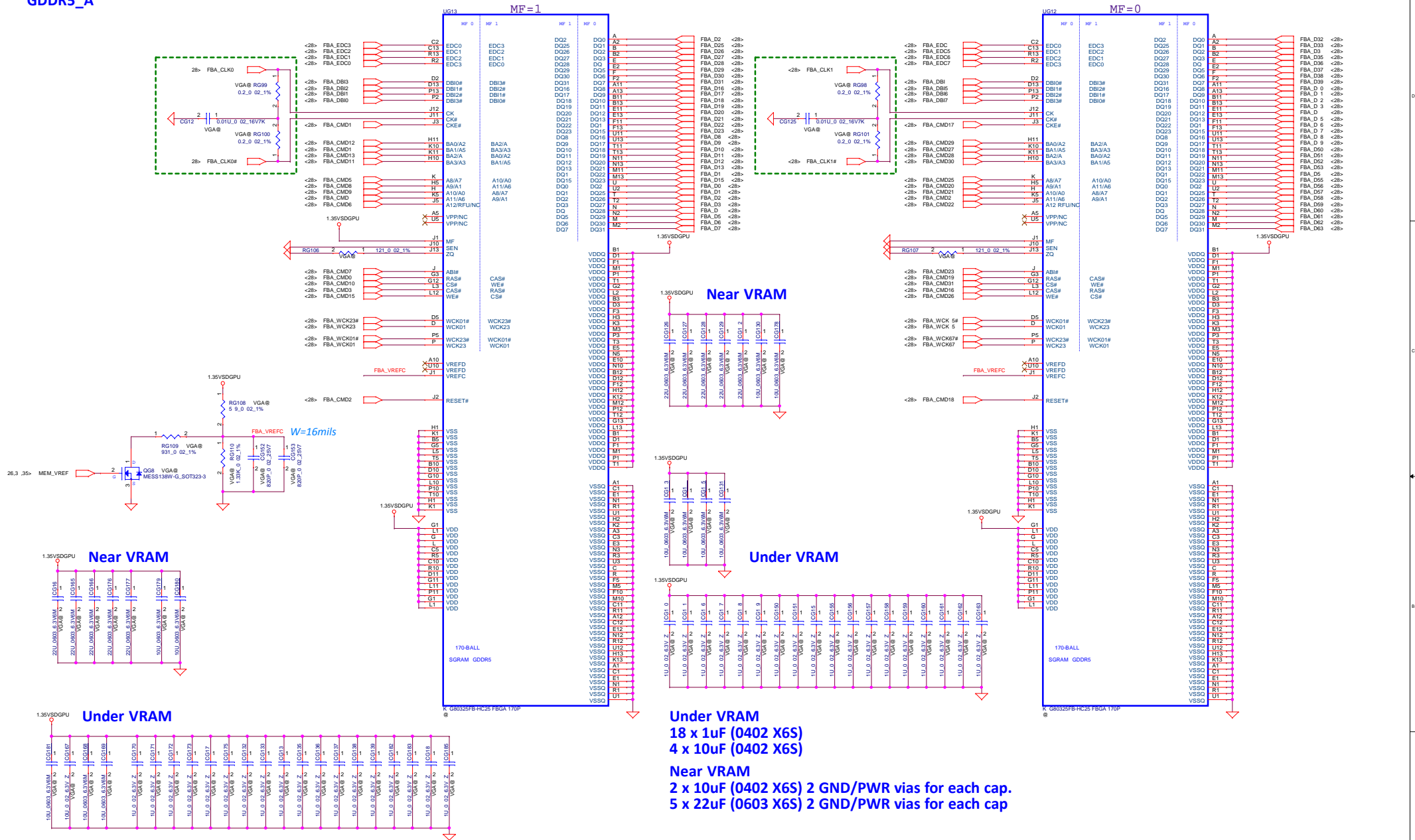
Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	



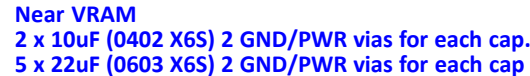
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/12/15	Deciphered Date	2017/12/15	Title	N17E-G1(6/8) Strap Pin,ROM
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GDDR5_A

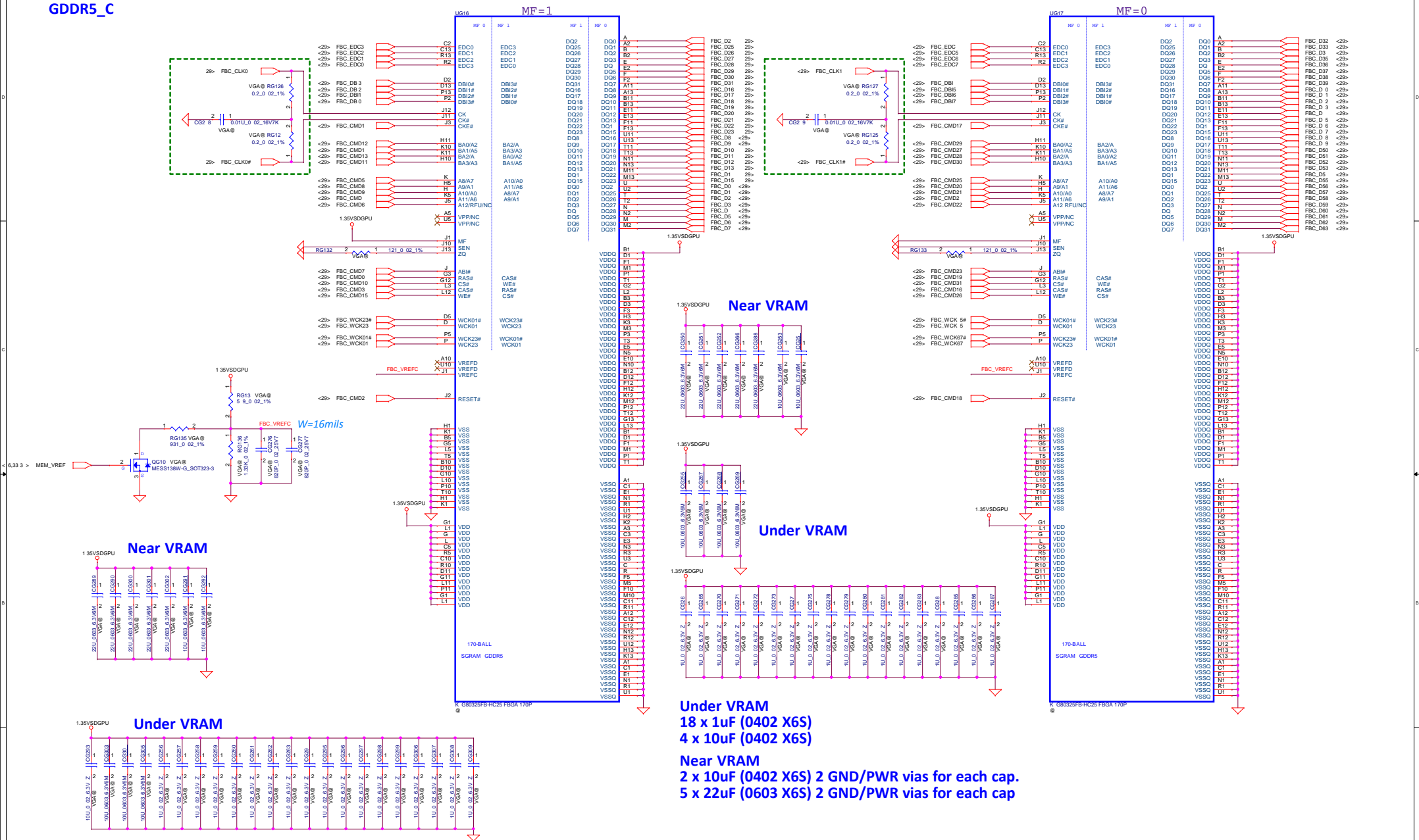


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			Rev 1A	
			DHD53F M/LA-F9P1P Drawn: 1/19/2018 13:01 Issue: 33 of 73	



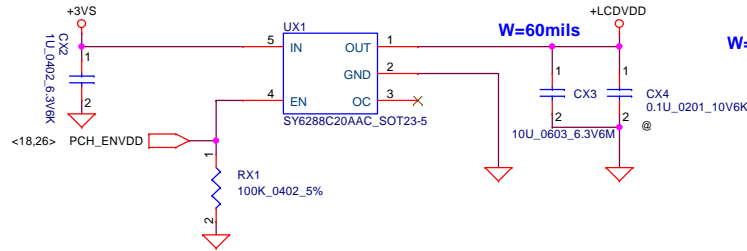
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GDDR5_C

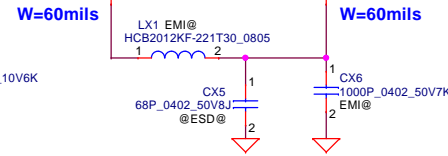


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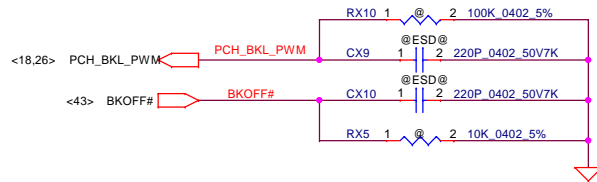
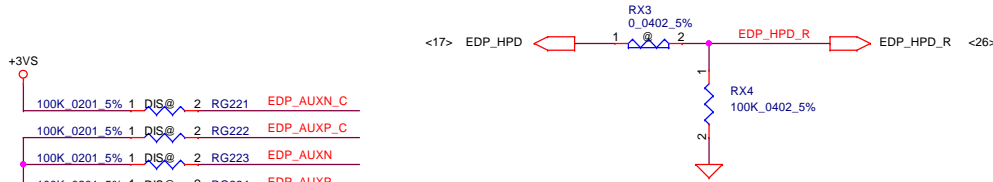
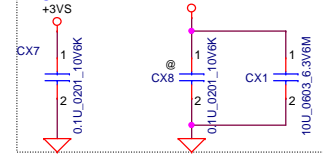
LCD POWER CIRCUIT



SM01000EJ00 3000ma
220ohm @ 100mhz
DCR 0.04



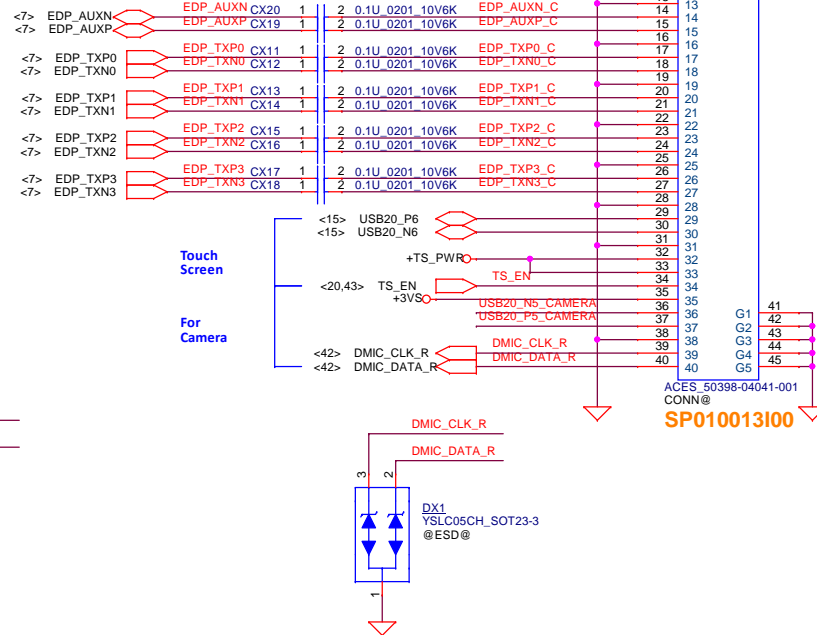
Place closed to
JEDP1



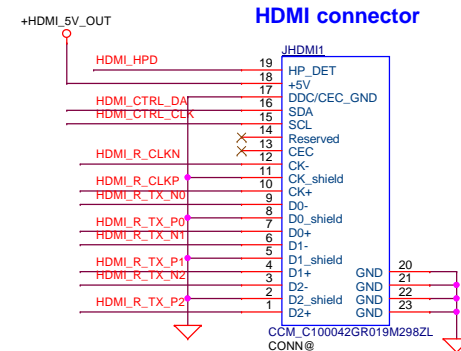
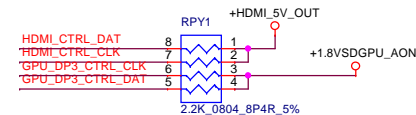
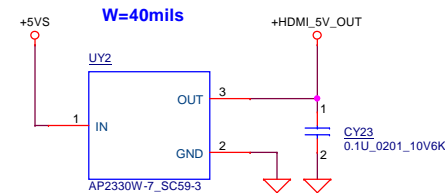
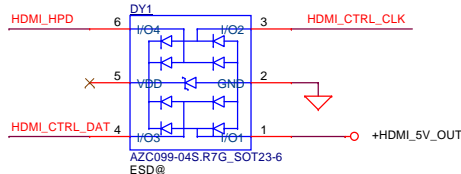
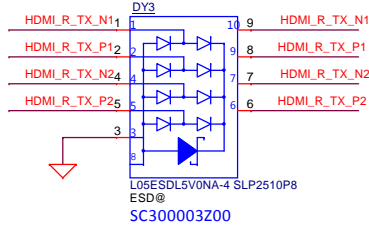
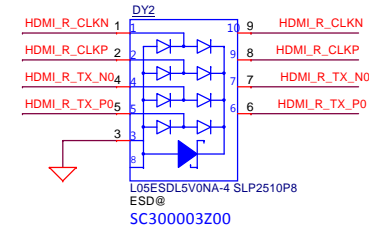
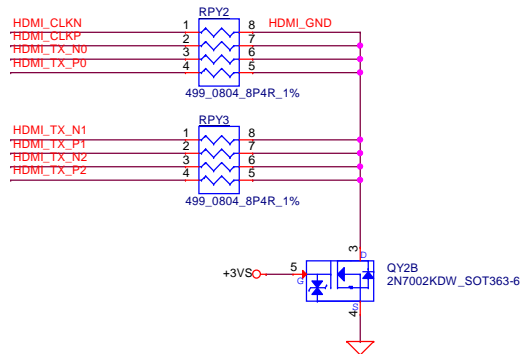
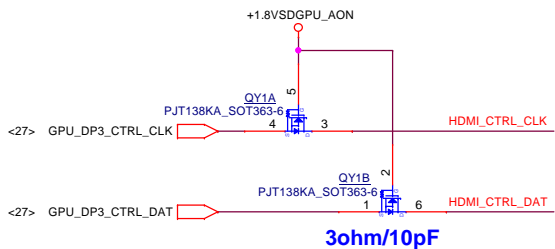
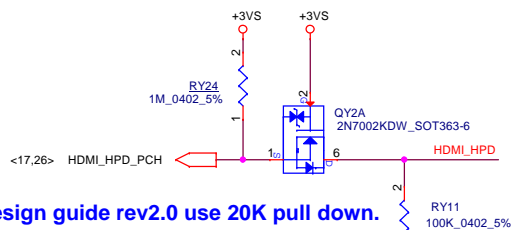
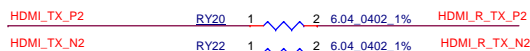
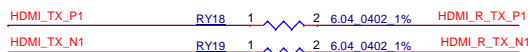
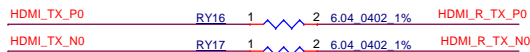
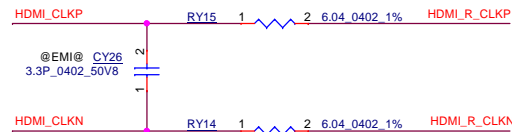
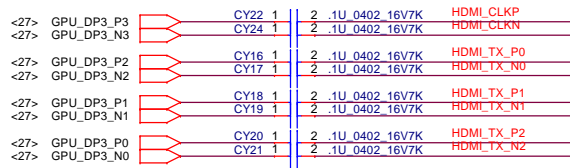
USB Touch Screen



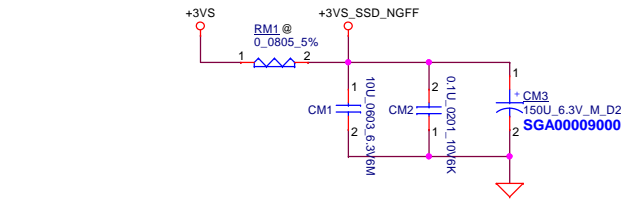
Camera



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<18> PCIE_PRX_DTX_N9
<18> PCIE_PRX_DTX_P9

<18> PCIE_PTX_DRX_N9
<18> PCIE_PTX_DRX_P9

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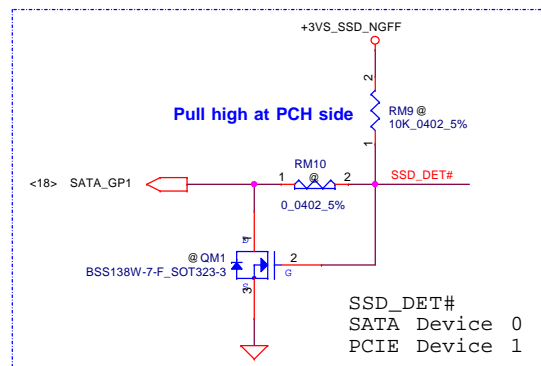
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CM4 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_P9

CM5 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_N10
CM7 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_P10

CM8 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_N11
CM9 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_P11

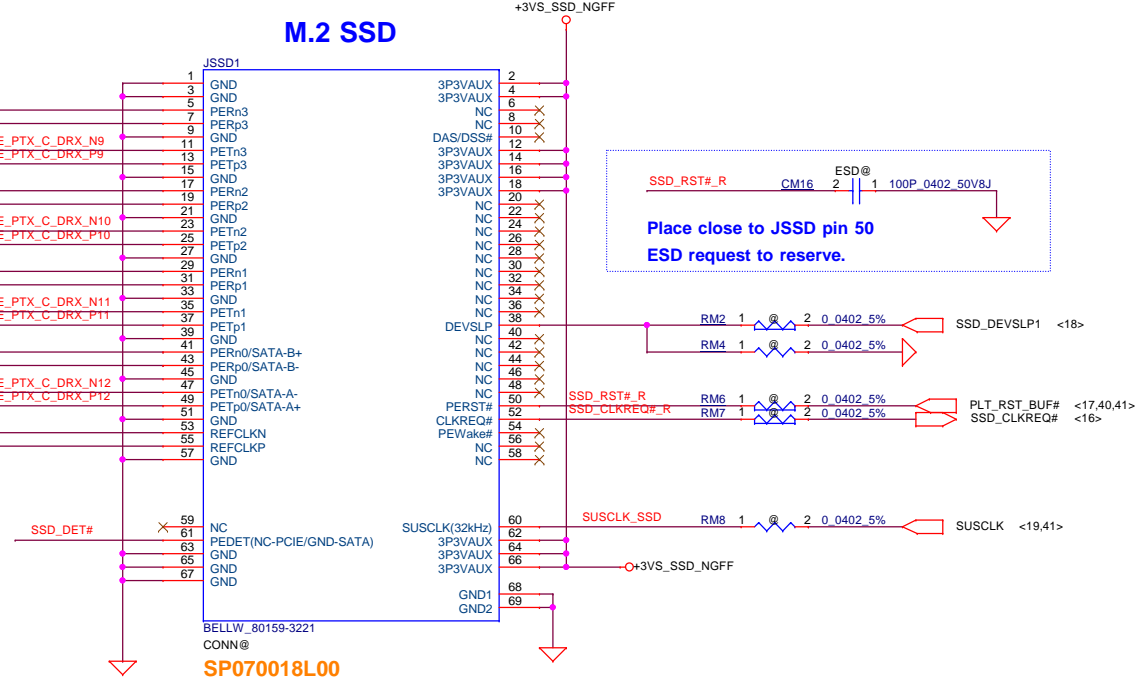
CM10 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_N12
CM11 1 2 0.22U 0402 16V7K PCIE_PTX_C_DRX_P12



<18> SATA_GP1

SSD_DET#
SATA Device 0
PCIE Device 1

M.2 SSD



SSD_RST#_R CM16 2 1 100P_0402_50V8J
Place close to JSSD pin 50
ESD request to reserve.

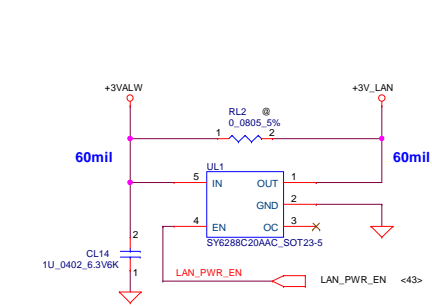
SSD_RST#_R RM6 1 2 0 0402 5% PLT_RST_BUF# <17,40,41>
SSD_CLKREQ#_R RM7 1 2 0 0402 5% SSD_CLKREQ# <16>

SUSCLK_SSD RM8 1 2 0 0402 5% SUSCLK <19,41>

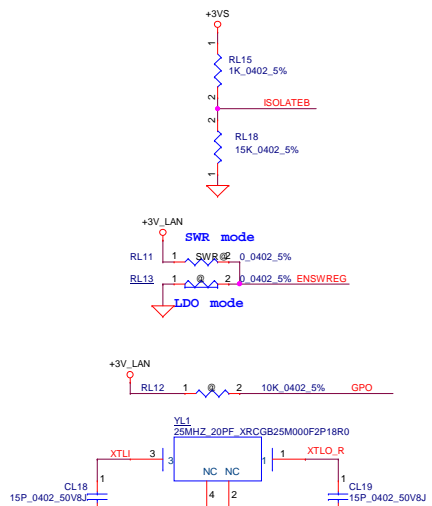
SSD_RST#_R 2 1 10K_0402_5% +3VS
SSD_CLKREQ#_R 2 1 10K_0402_5% +3VS
reserve for Optane Memory

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Size	Document Number	Rev		1.A	
Custom	DH53F M/B LA-F991P	Date		Tuesday February 13 2018	
Sheet		39		of 73	

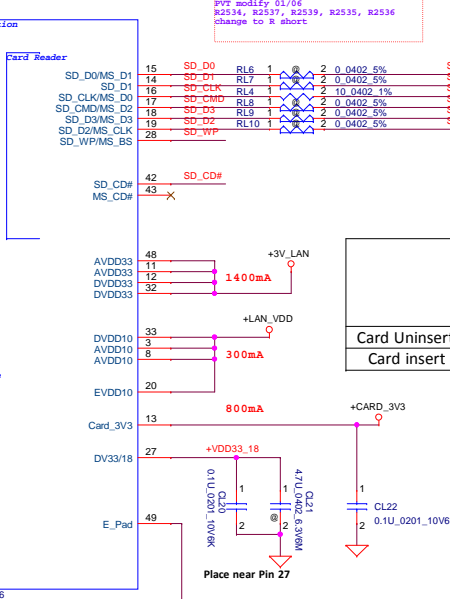
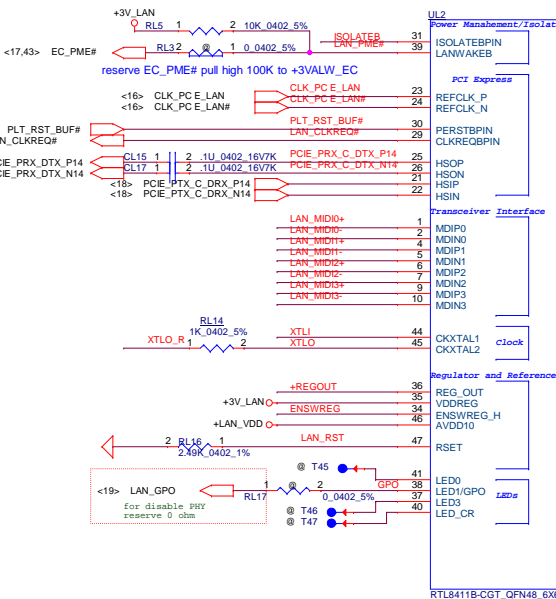
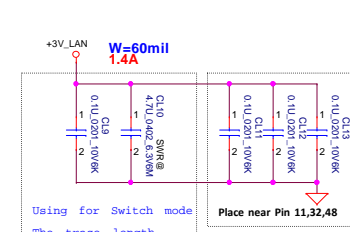
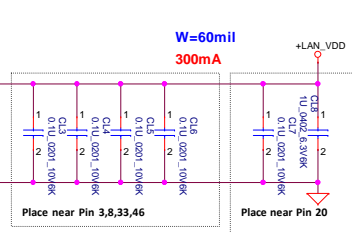
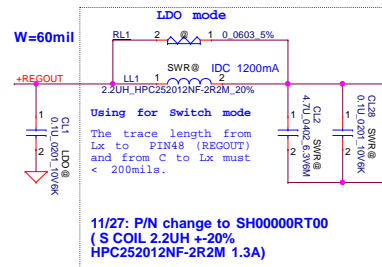
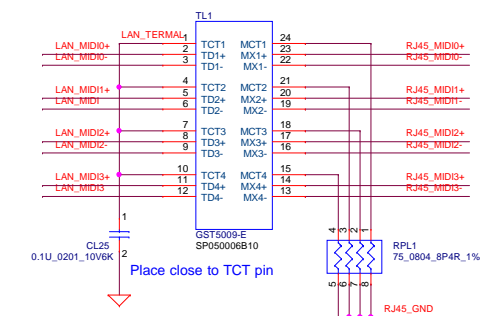
LAN-RTL8411B



From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms

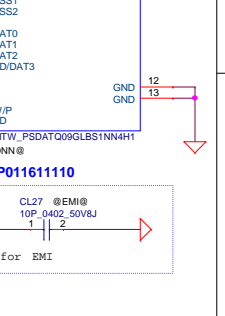
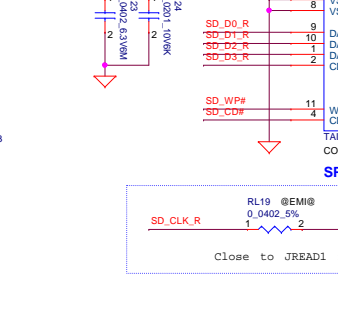
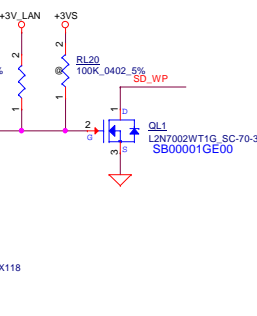
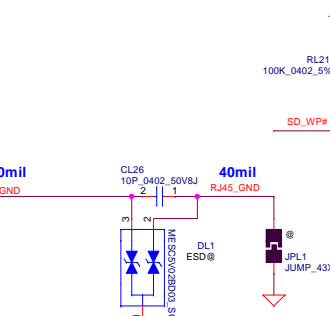
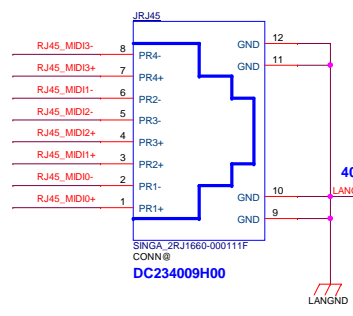


P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



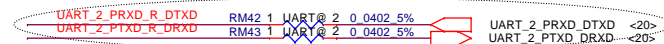
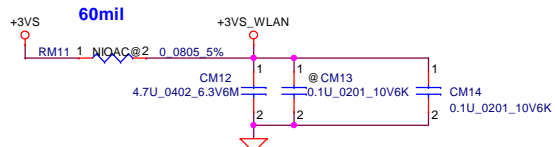
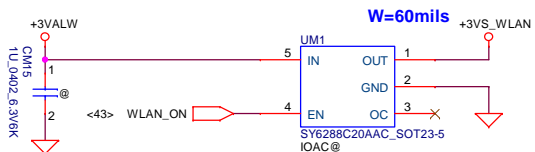
	Protect cotact	Card contact
Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open
Card insert	Open	Close

LAN Connector



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Title		LAN RTL8411H	
Size	Document Number	Rev 1A	
Customer	DH53F M/B LA-F991P		
Date	Tuesday February 13 2018	Sheet	40 of 73

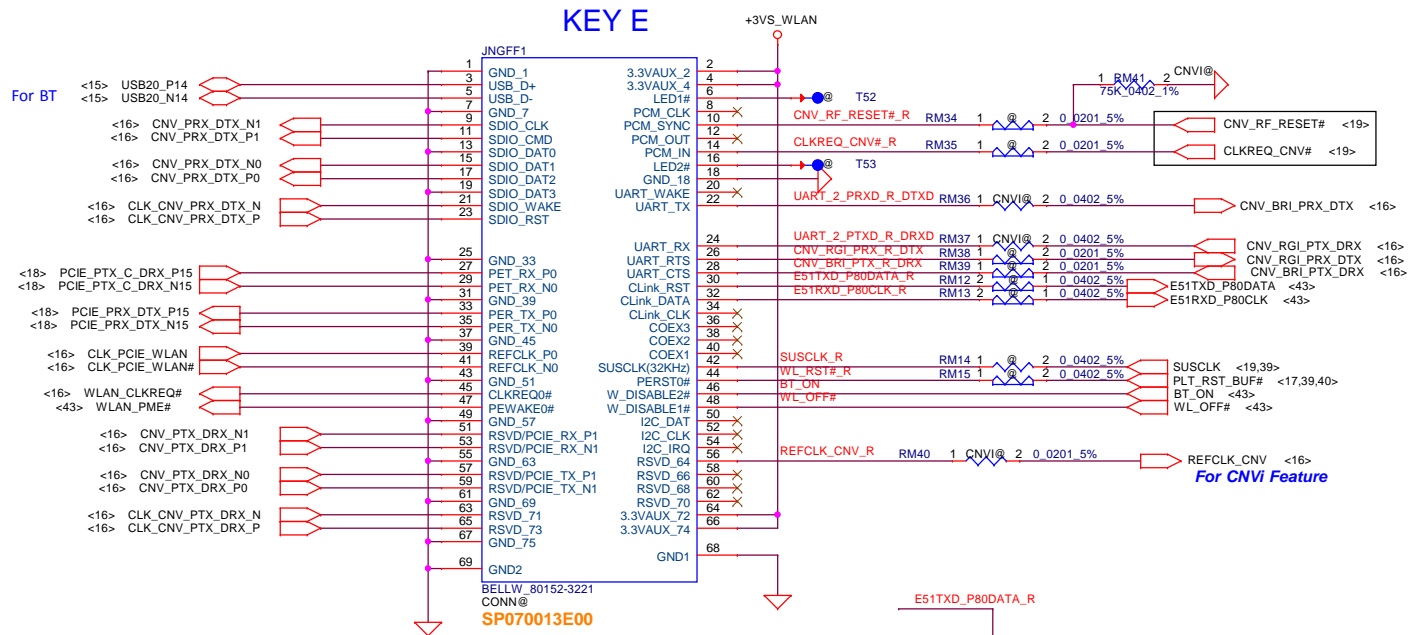
Wireless LAN



Co-layout with CNVi

PH +3VS at SOC side,
for win7 USB3 debug

KEY E

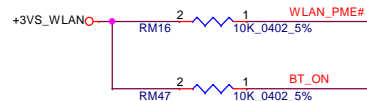


NGFF WL+BT (KEY E)

74	1.0	GND	75
76	1.0	RESERVED/REFCLK1	73
72	1.0	RESERVED/REFCLKP1	71
70	UM_Power_SPC/GPIO/PFWake#	GND	69
68	UM_Power_SNN/CLKREQ2	Reserved/PERP1	67
66	UM_SW/PERST#	Reserved/PERP1	65
64	RESERVED	GND	63
62	ALERT# (I/O)(3.3)	Reserved/PTN1	61
60	QCC CLK (I/O)(3.3)	Reserved/PTP0	59
58	QCC DATA (I/O)(3.3)	GND	57
56	W_DISABLE#1 (O)(0.9V)	PERWake#1 (O)(0.9V)	55
54	Reserved#V_DISABLE2 (O)(0.9V)	CLKREQ# (O)(0.9V)	53
52	PERSTW (I/O)(3.3V)	GND	51
50	SUSCIN(20MHz) (O)(0.9V)	REFCLK0	49
48	CODE1 (I)(O)(1.8V)	REFCLKP0	47
46	CODEX3 (I)(O)(1.8V)	GND	45
44	CODEX3 (I)(O)(1.8V)	PER#0	43
42	VENDOR DEFINED	PER#0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PTN#0	37
36	UART RTS (I/O)(1.8V)	PETP0	35
34	UART CTS (I)(O)(1.8V)	GND	33
32	UART Tx (I/O)(1.8V)	Reserved#V_DISABLE2 (O)(0.9V)	
22	UART Rx (I/O)(3.3V)	SDIO Reset# (O)(0.9V)	23
20	UART Wake# (I)(O)(3.3V)	SDIO Wake# (I)(O)(1.8V)	21
18	GND	SDIO DAT[7:0] (I/O)(1.8V)	19
16	LED#2 (I)(I/O)	SDIO DAT[7:0] (O)(1.8V)	17
14	PCM_OUT/IS2_HS_OUT (I/O)(1.8V)	SDIO DAT[3:0] (I/O)(1.8V)	15
12	PCM_IN/IS2_HS_IN (I/O)(1.8V)	SDIO DAT[7:0] (O)(1.8V)	13
10	PCM_SYNC/IS2_HS (O)(1.8V)	SDIO CMD[0] (I/O)(1.8V)	11
8	PCM_CLK/IS2_SCK (O)(1.8V)	SDIO CLK (I/O)(1.8V)	9
6	LED#1 (I)(I/O)		
4	1.0	USB_D-	5
2	1.0	USB_D+	3
		GND	1

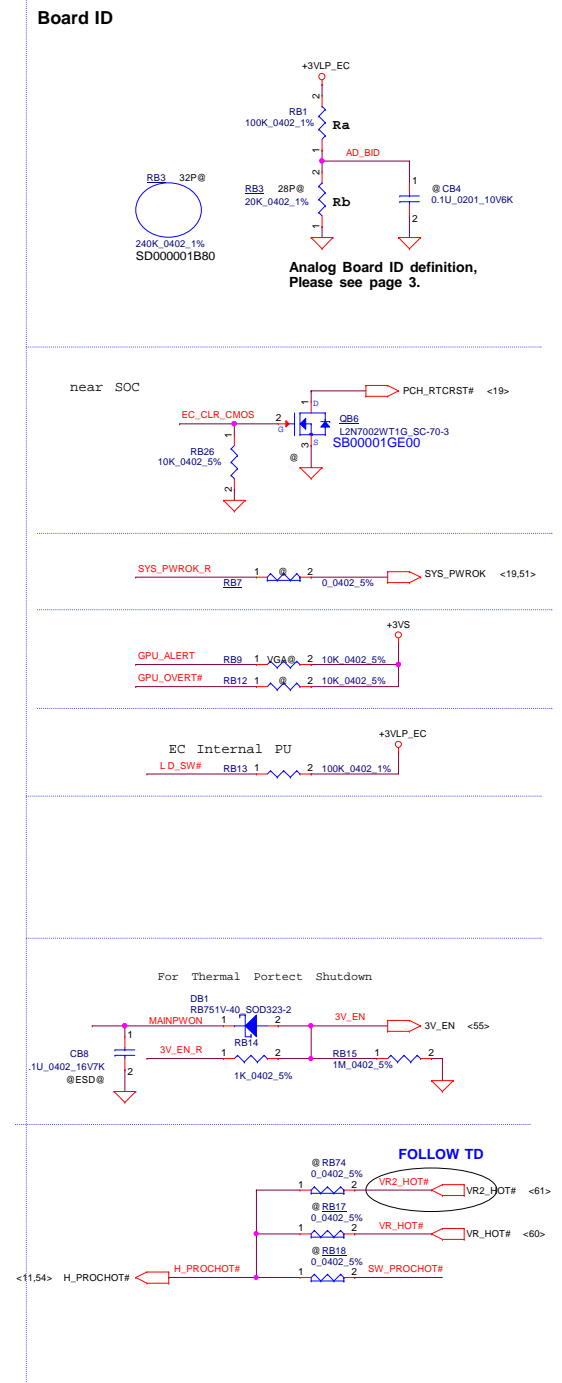
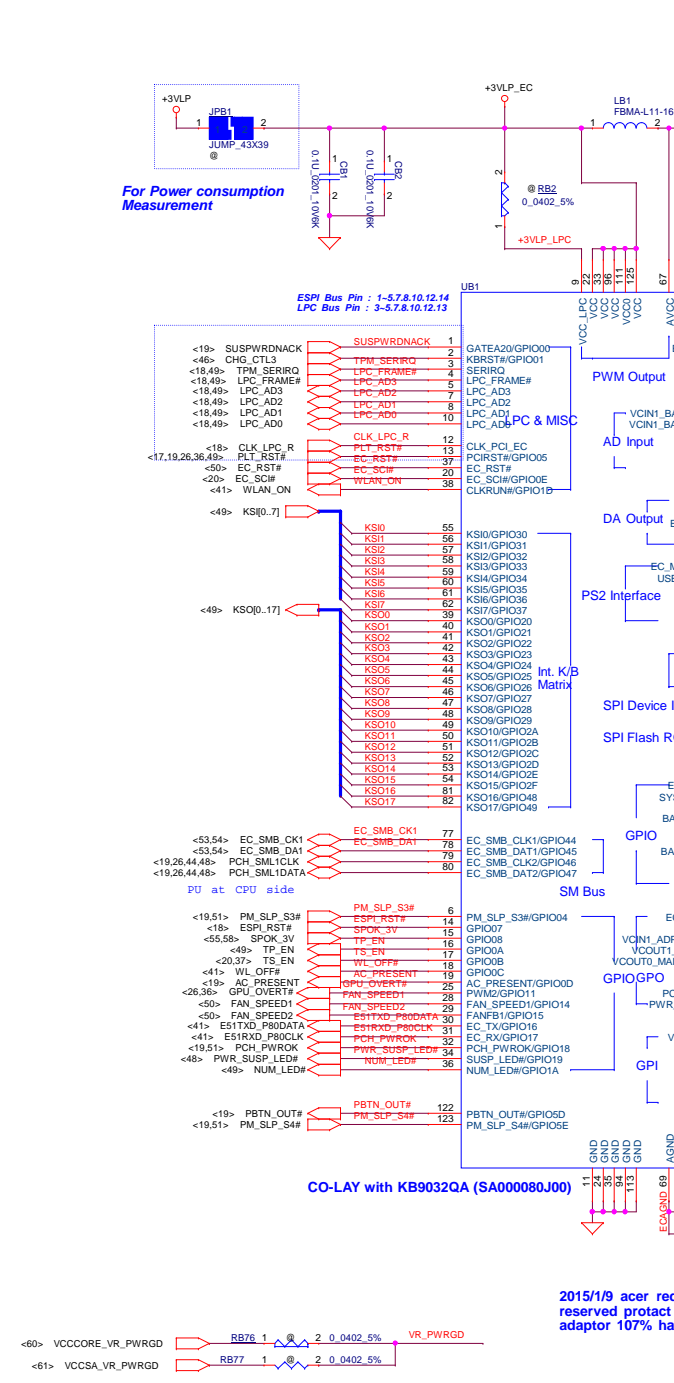
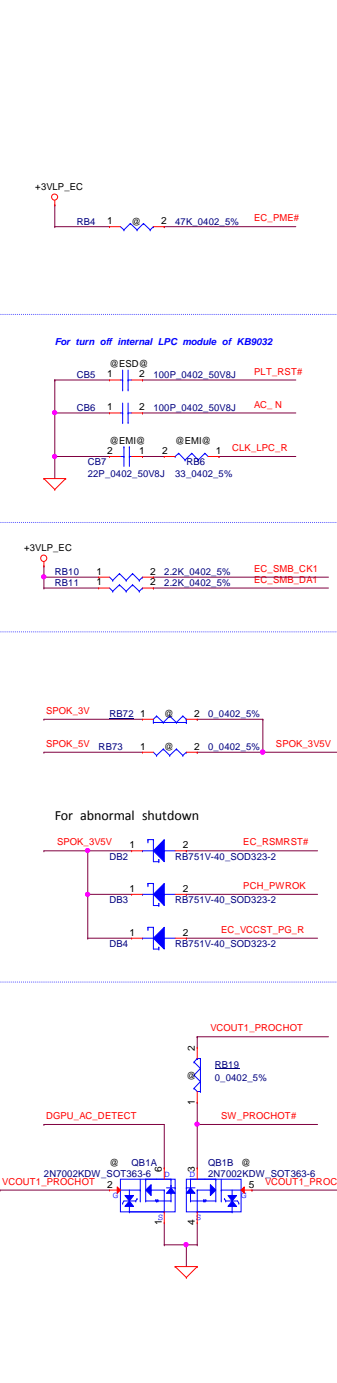


(From PCH CLKOUT2)
PCIE CLK



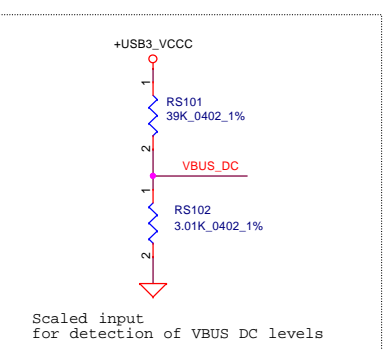
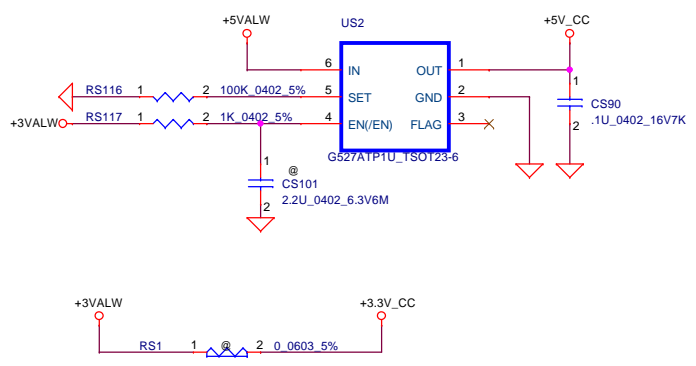
For CNVi Card

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				Size	Document Number	Rev
				DH53F M/B LA-F991P		
Date	Tuesday February 13 2018	Sheet	41	of	73	1.A



2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen

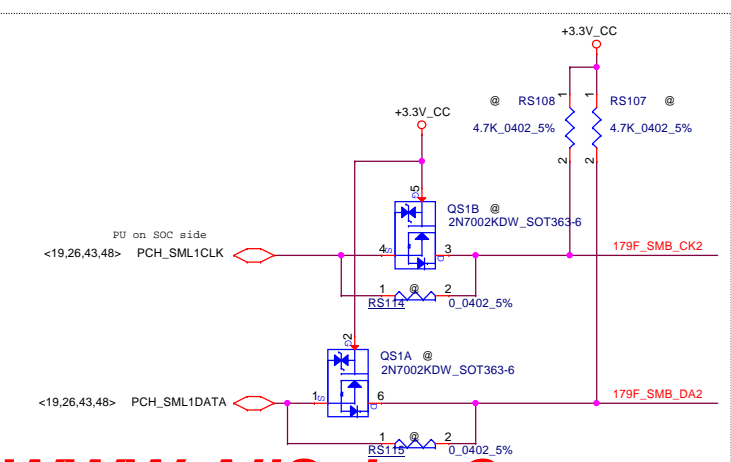
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Tite		Ene ENE-KB9012A4/KB9022	
Size		Custom	
Date		Tuesday February 13 2018	
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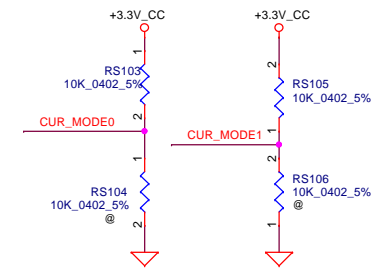
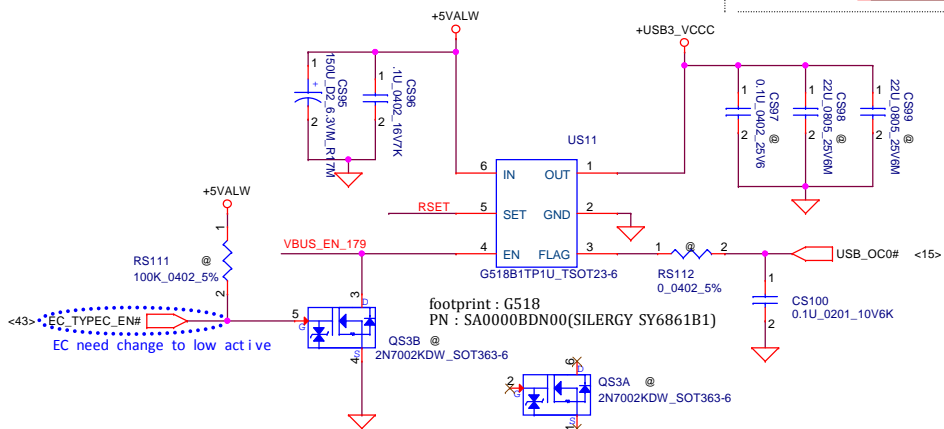
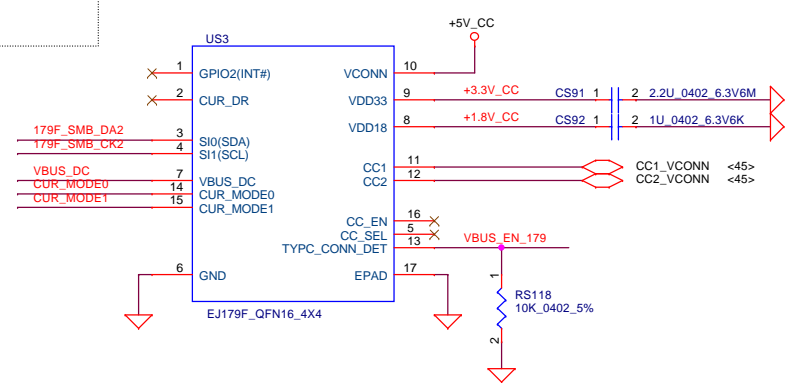
Remove INT#, platform doesn't monitor it

report CC1 or CC2 is connection

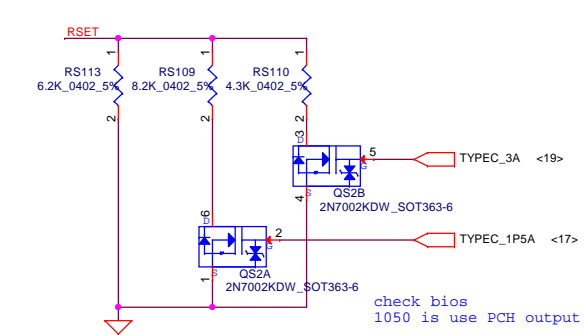
CC_EN power path control "low active"



WWW.AliSaler.Com



Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current

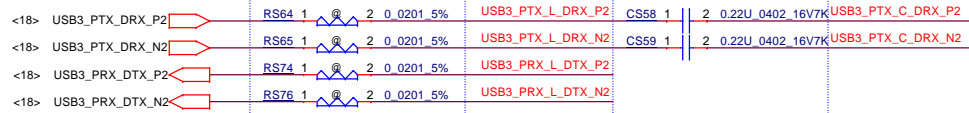


G518 MOS Current Limit				
GPP_B1 TYPEC_1P5A	GPP_B4 TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

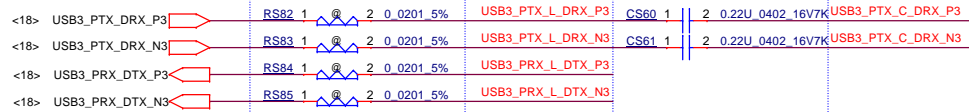
Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

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Size Custom	Document Number	Date		Rev	
	DH53F M/B LA-F991P	Tuesday February 13 2018		1A	
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USB3.0 (Port 2)

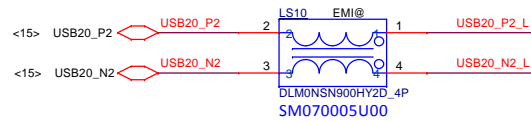


USB3.0 (Port 3)

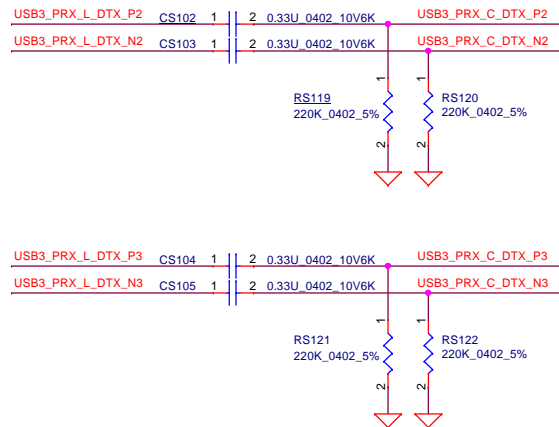
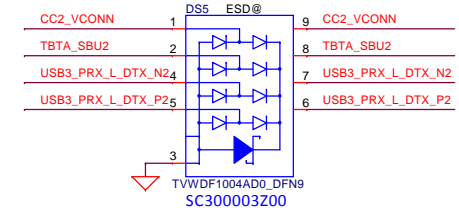
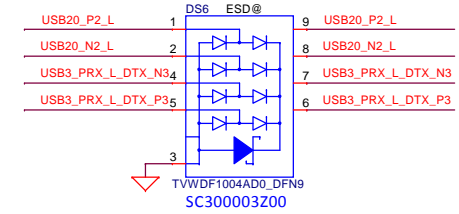
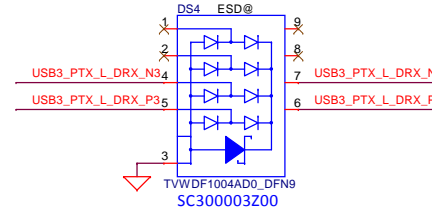
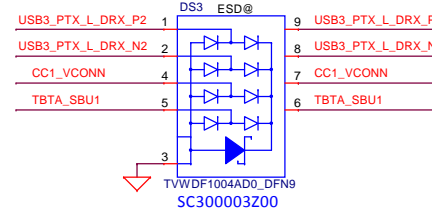


Change to 0201 for placement.

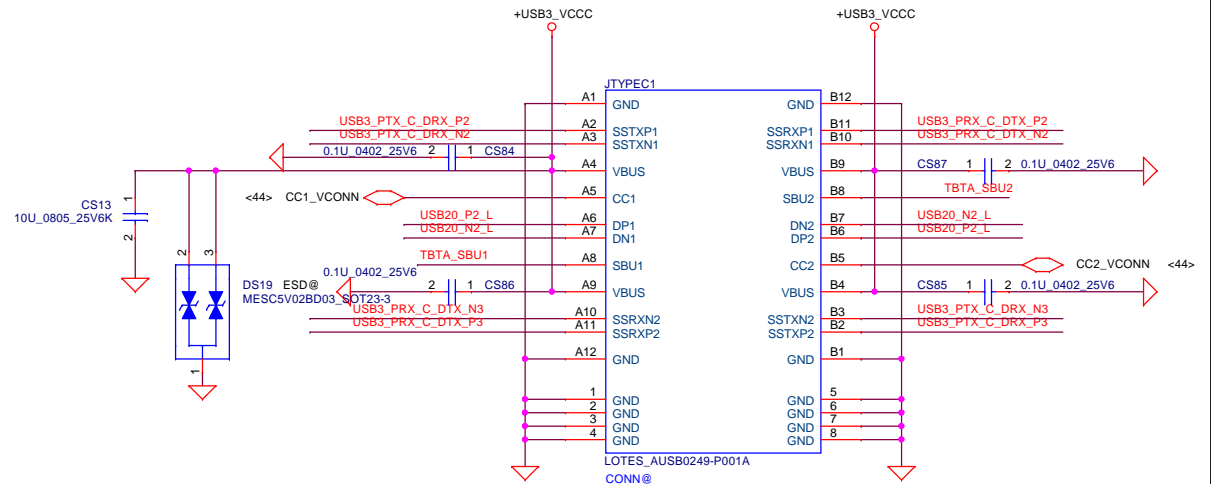
Follow intel #575549.



For ESD request



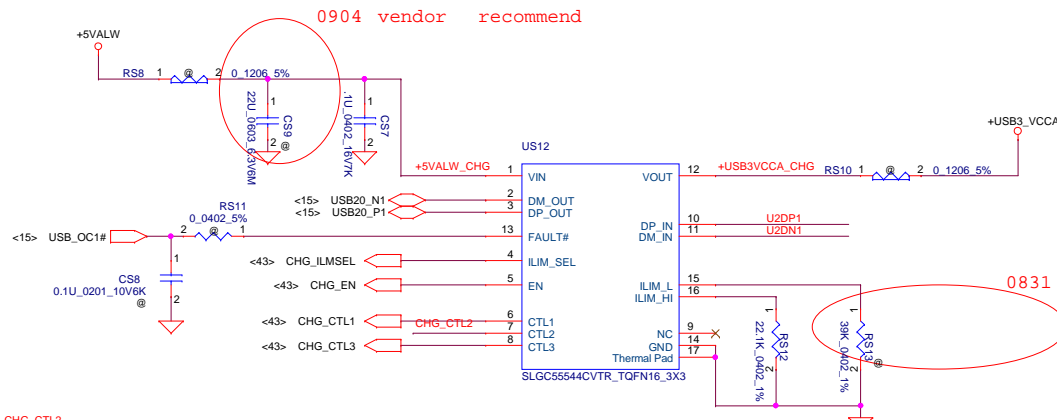
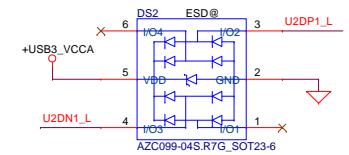
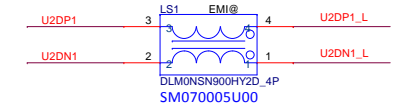
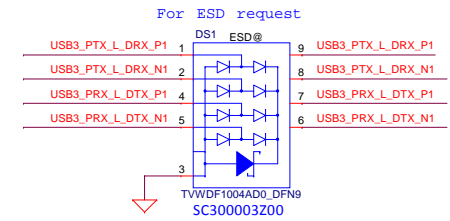
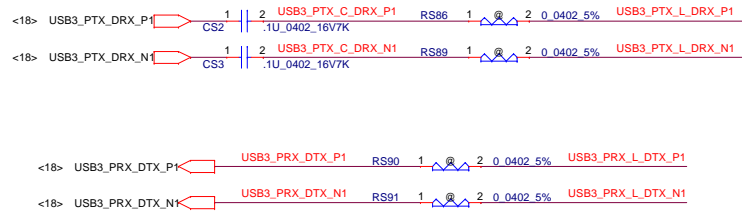
Follow intel #575549 for ESD/EOS protection.



CC1_VCONN & CC2_VCONN need 20mil trace width.

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USB3.0



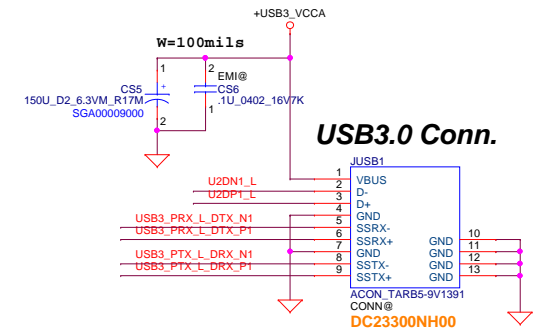
0831 Reserve ILIM_L R as vendor recommend

ILM R vaule
 $I_{os} (mA) = 50250 / R (Kohm)$
 $ILIM_Hi = 2273mA$
 $ILIM_L = 1288mA (reserve)$

0831 Rerserve PU, check if SDP1 mode is need, just PU if no need

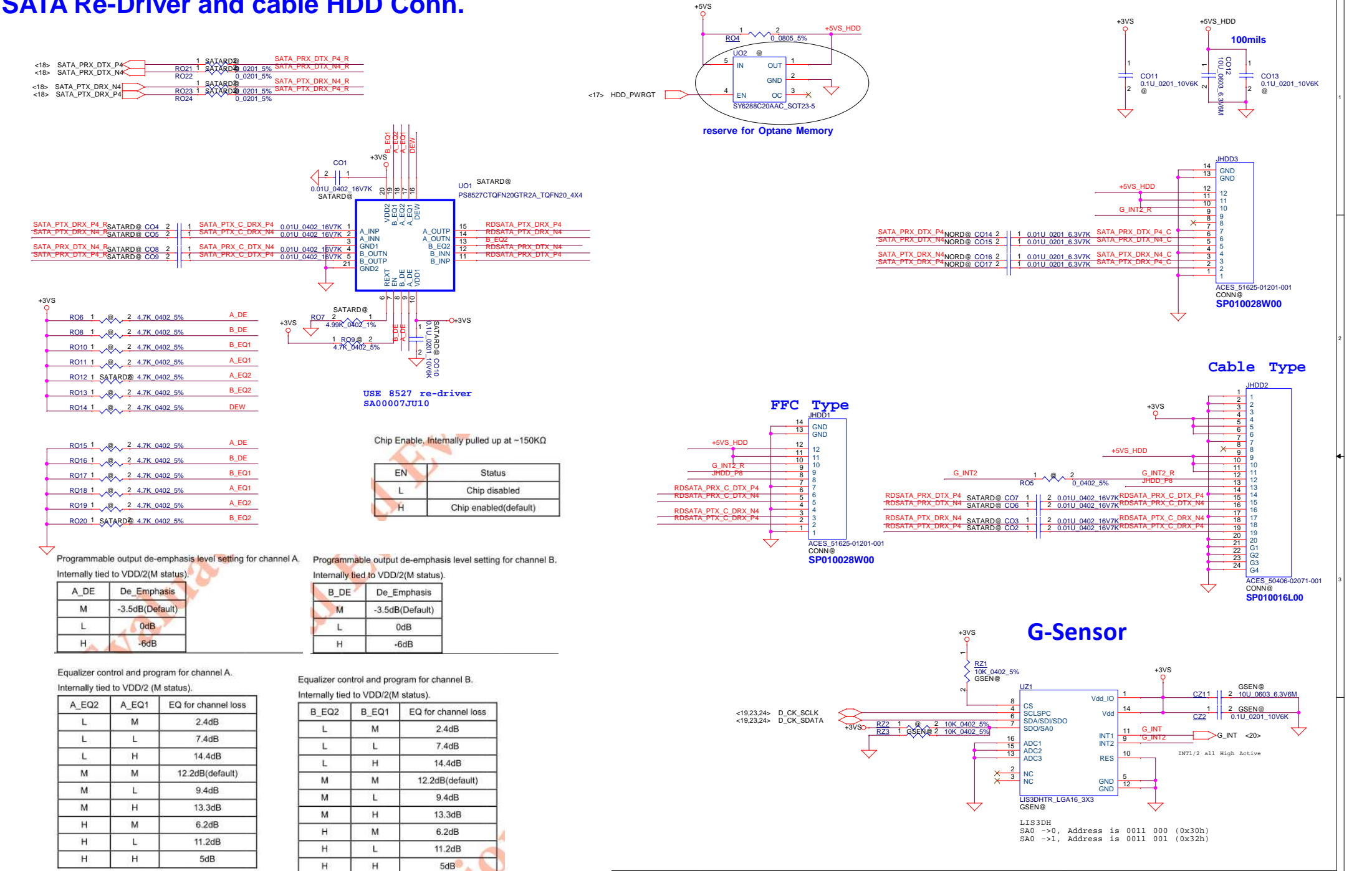
USB Host Charger

CTL1	CTL2	CTL3	ILIM SEL	MODE	Current Limit Setting	Note
1	1	0	1	SDP1	ILIM H	Data Lines Connected
1	1	1	0	SDP2	ILIM L	Data Lines Connected
1	1	1	1	CDP	ILIM H	Data Lines Connected
0	1	1	1	DCP Auto	ILIM H	Data Lines Disconnected

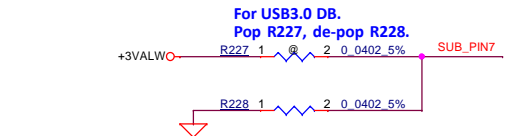
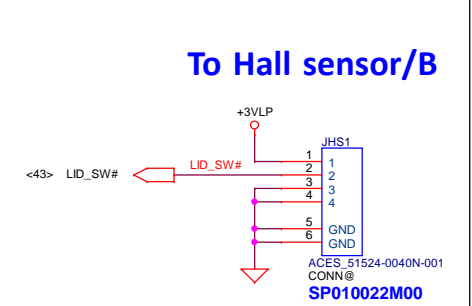
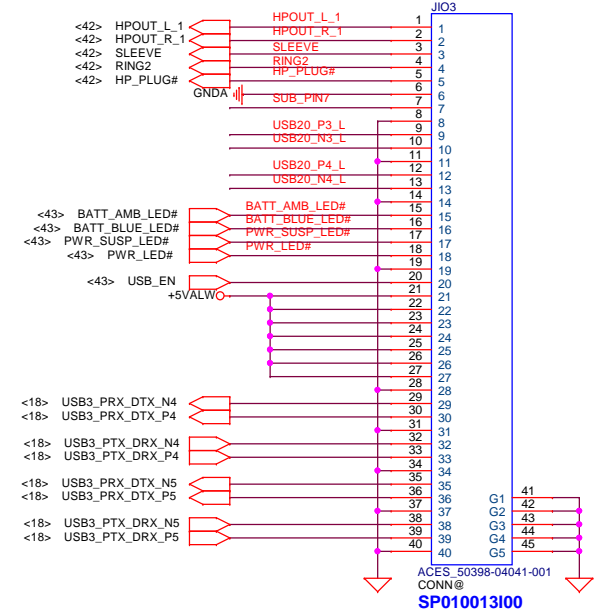
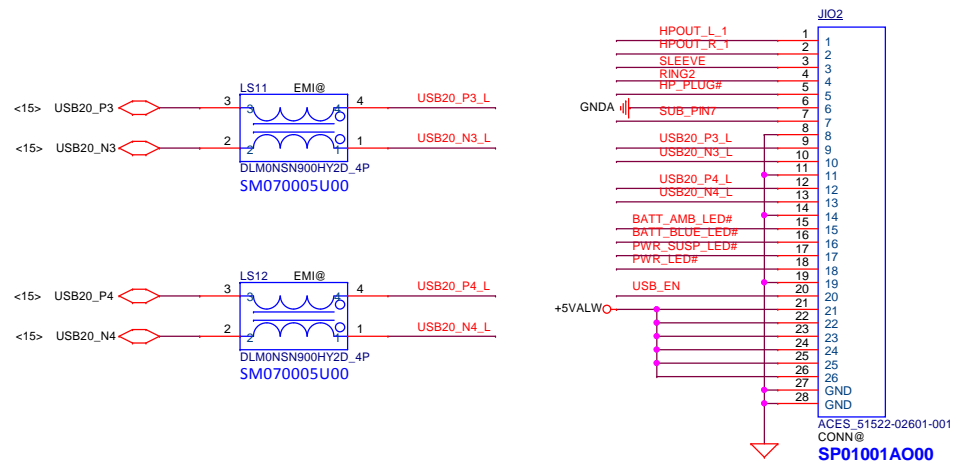


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						Size		Document Number		Rev	
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						DH53F M/B LA-F991P					

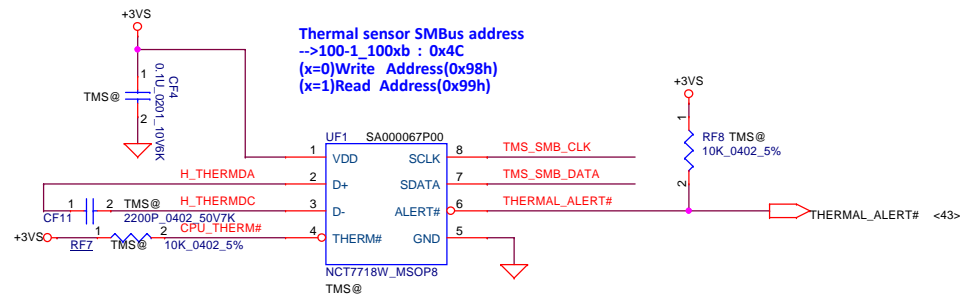
SATA Re-Driver and cable HDD Conn.



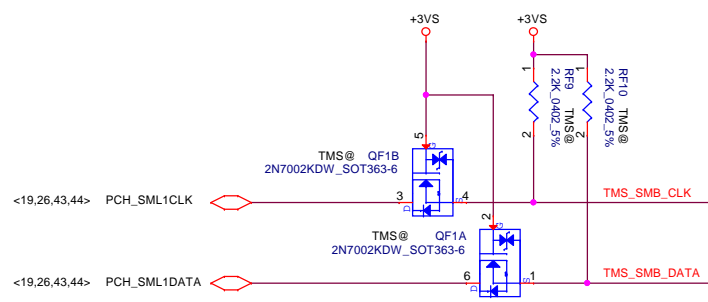
To USB/B FPC BTB CONN



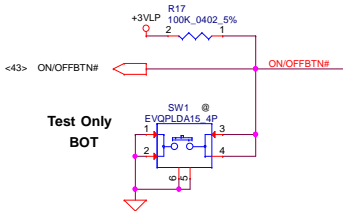
THERMAL SENSOR



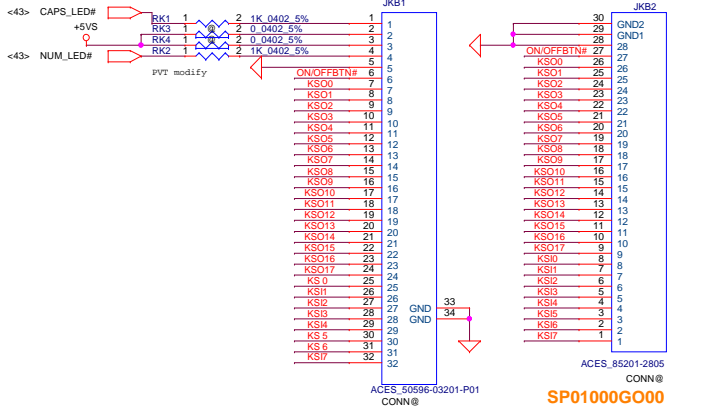
Thermal sensor SMBus address
->100-1_100xb : 0x4C
(x=0)Write Address(0x98h)
(x=1)Read Address(0x99h)



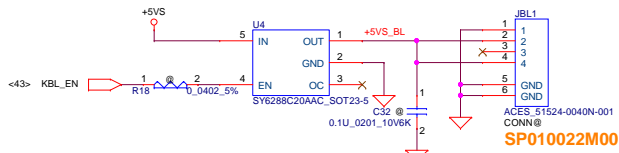
ON/OFF BTN



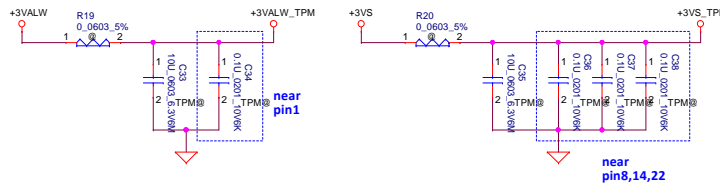
KB Conn.



KB BackLight

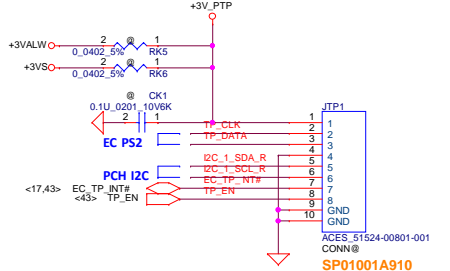
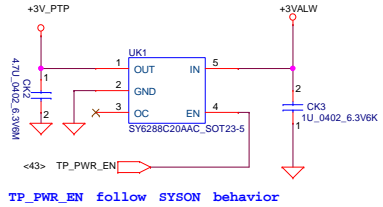


TPM

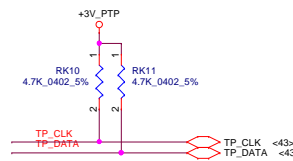
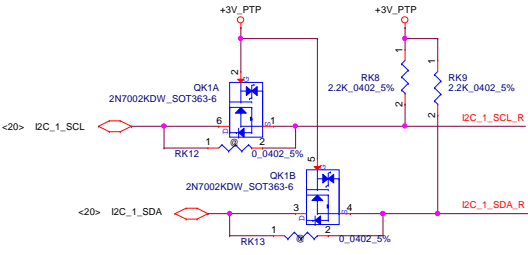


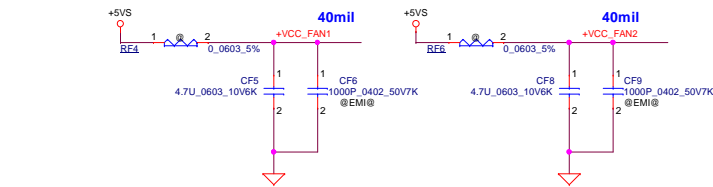
BADD	SELECTION
* 1	Aeh(write), Afh(read)

Touch Pad

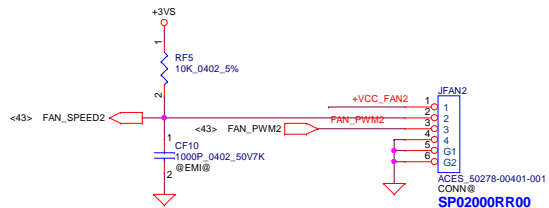
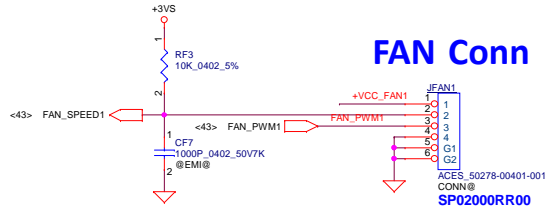


SERIRQ PH 10K to +3VS at PCH side
CLKRUN# PH 10K to +3VS at PCH side
LPCPD# had internal PH

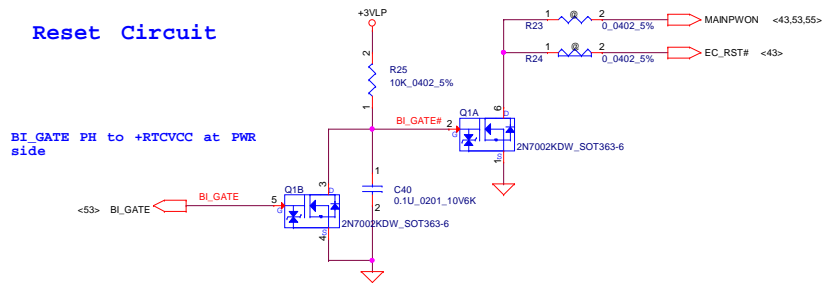




FAN Conn



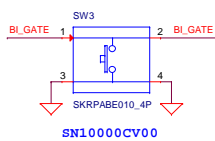
Reset Circuit



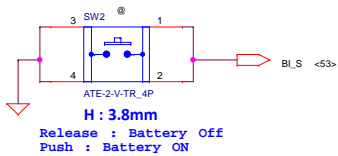
BI_GATE PH to +RTCVCC at PWR side

<53> BI_GATE

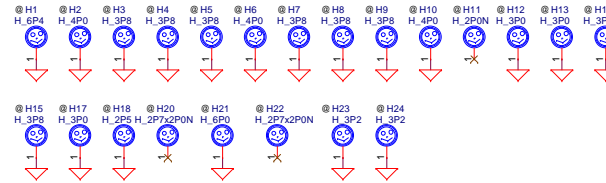
Reset Button



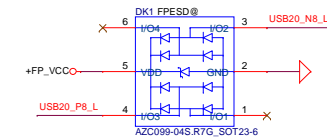
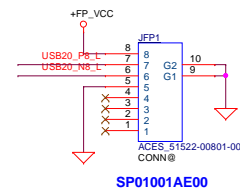
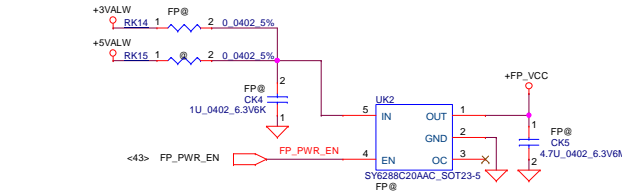
BI SW



Screw Hole



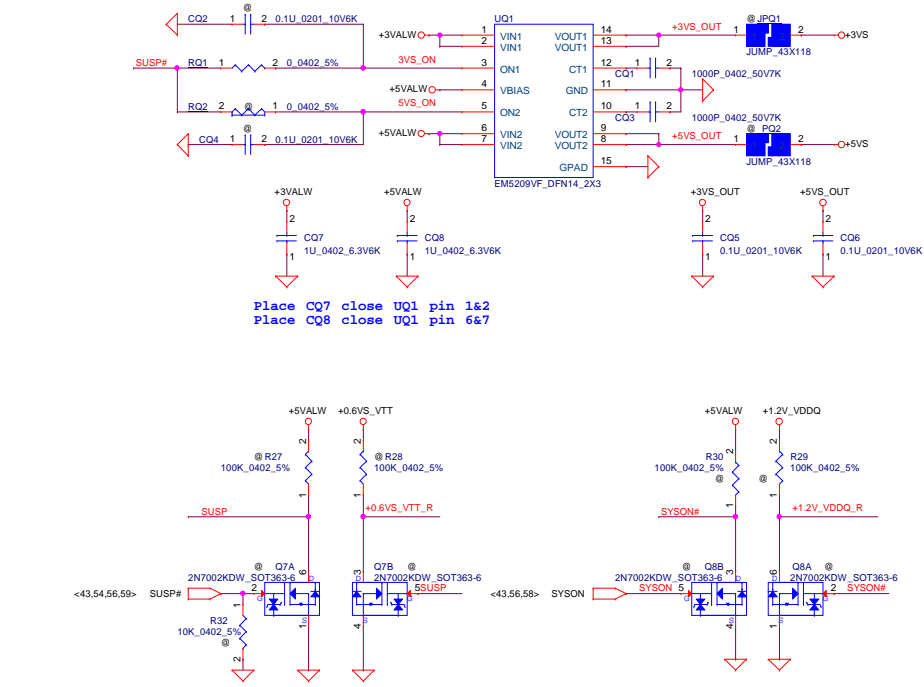
Finger Print



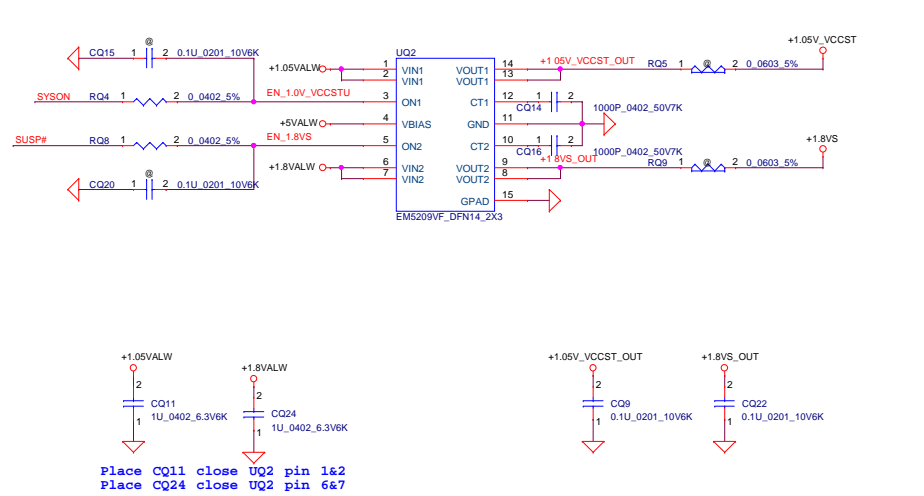
PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

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				Date	Tuesday, February 13 2018	Sheet 50 of 73

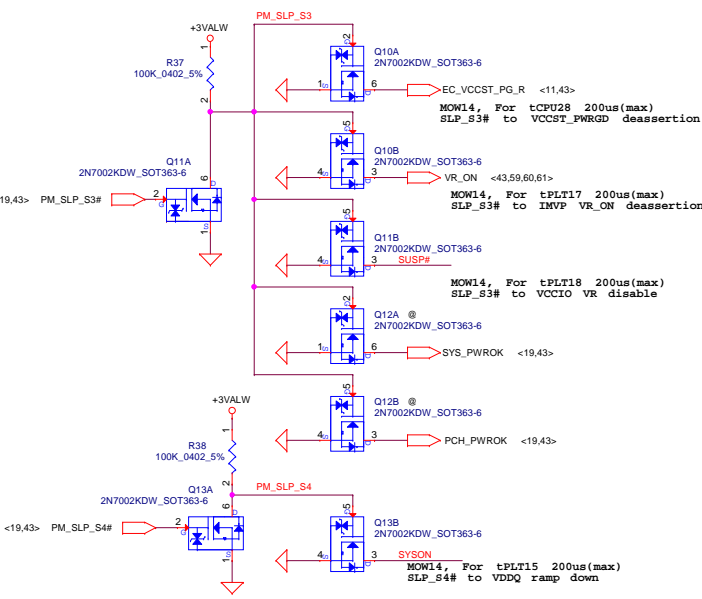
System DC interface



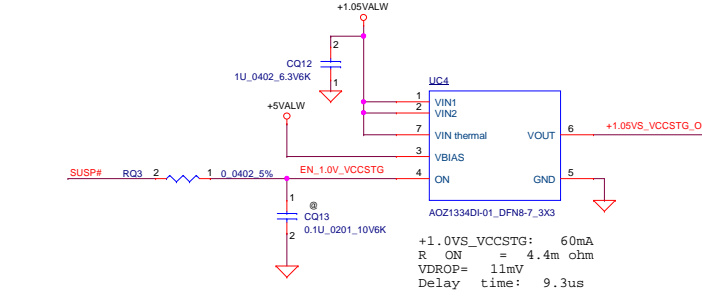
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



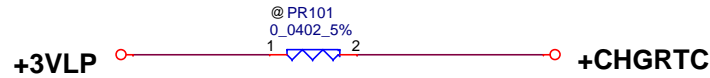
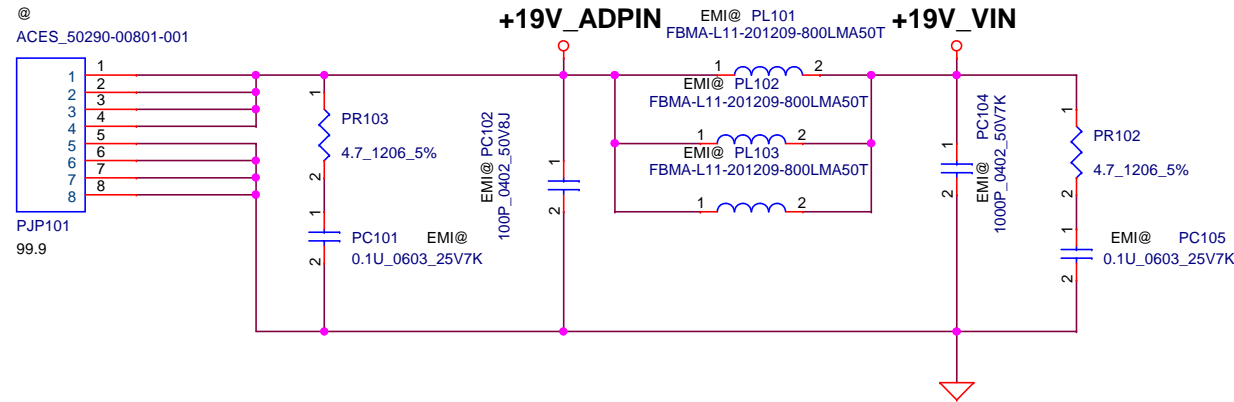
For Power ON/Off Sequence



+1.05VALW TO +1.05VS_VCCSTG



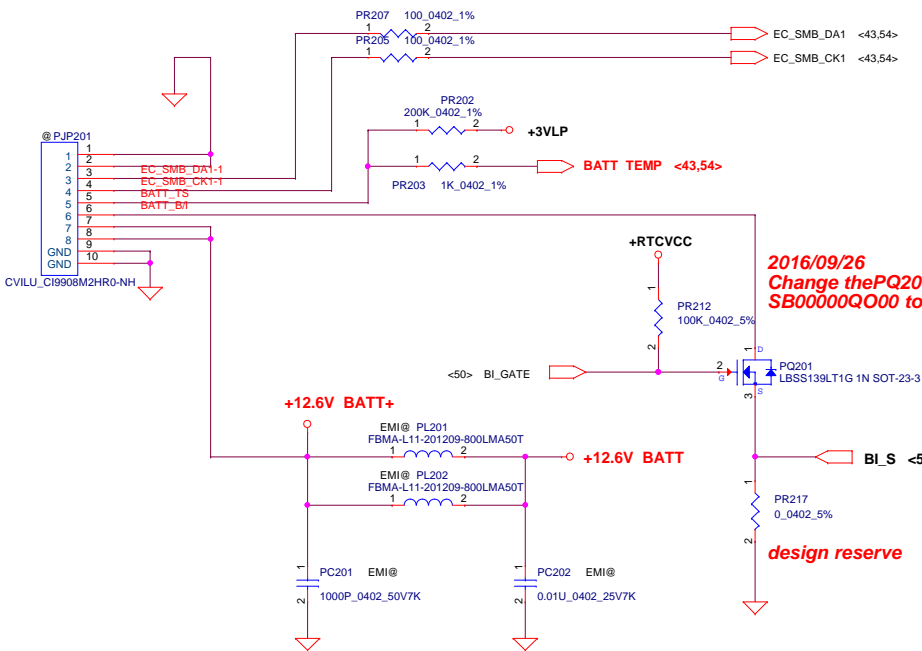
change PL101 PL102 PL103 from
M01000P200 to SM01000U600



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Battery Bot Side

- PIN1 GND
- PIN2 GND
- PIN3 SMD
- PIN4 SMC
- PIN5 TEMP
- PIN6 BI
- PIN7 Batt+
- PIN8 Batt+



2016/09/26
Change the PQ201 from
SB00000Q000 to SB00001GD00,

design reserve

<45, 47>
<43,50,55> MAINPWON

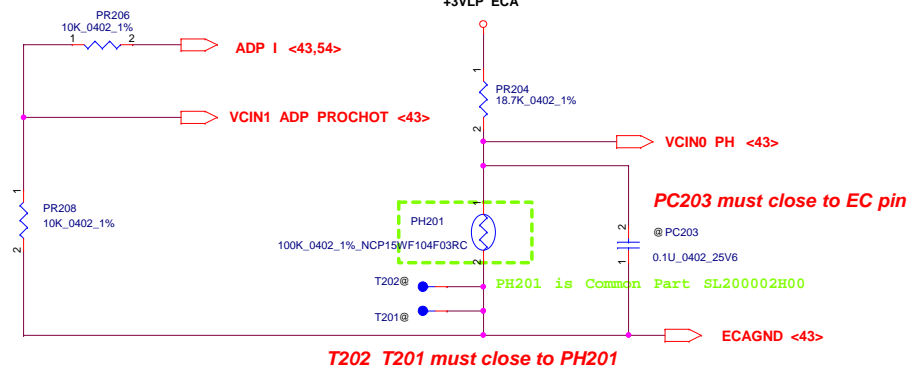
2016/11/22 update

For KB9022 sense 5mΩ	Active	Recovery

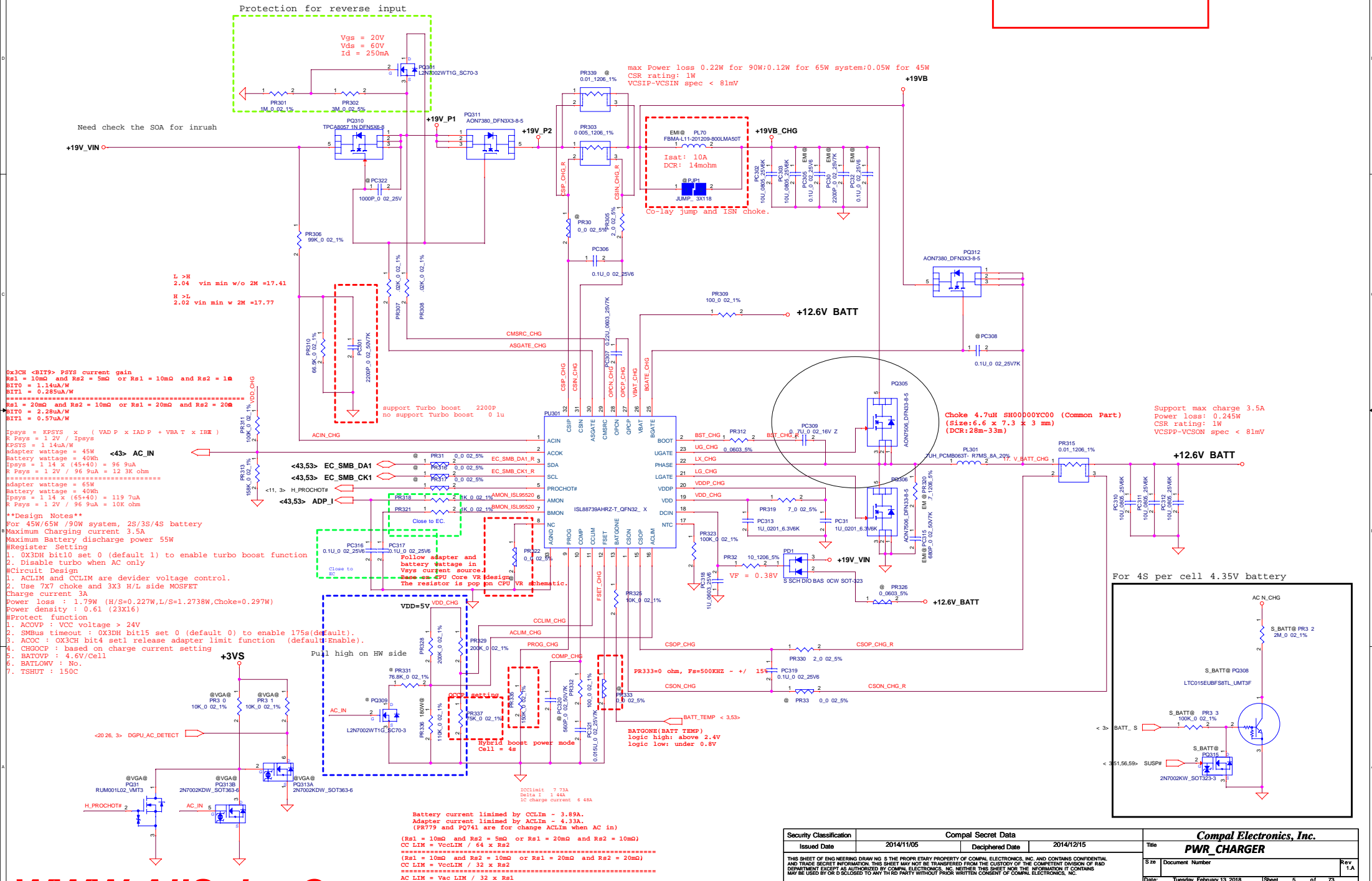
When PR204=16.9K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	89'C, 1V	56'C, 2V
PH202(ohm)	7.3092K	26.11K

3/27 thermal PH1 92'C ->89'C



$$ADP_I=20*I(adapter)*0.01$$
$$I(adapter)=adapter(W)*130\%/19$$



EN1 and EN2 don't floating

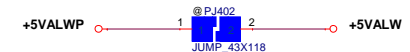
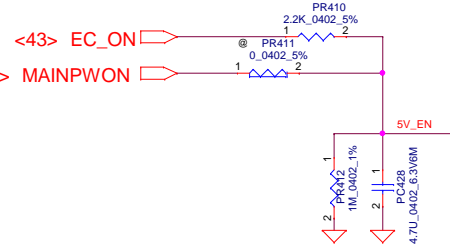
Check pull up resistor of SPOK at HW side

Choke 1.5uH SH000016800 (Common Part)
(Size:4.9 x 5.2 x 3 mm)
(DCR:20m-25m)

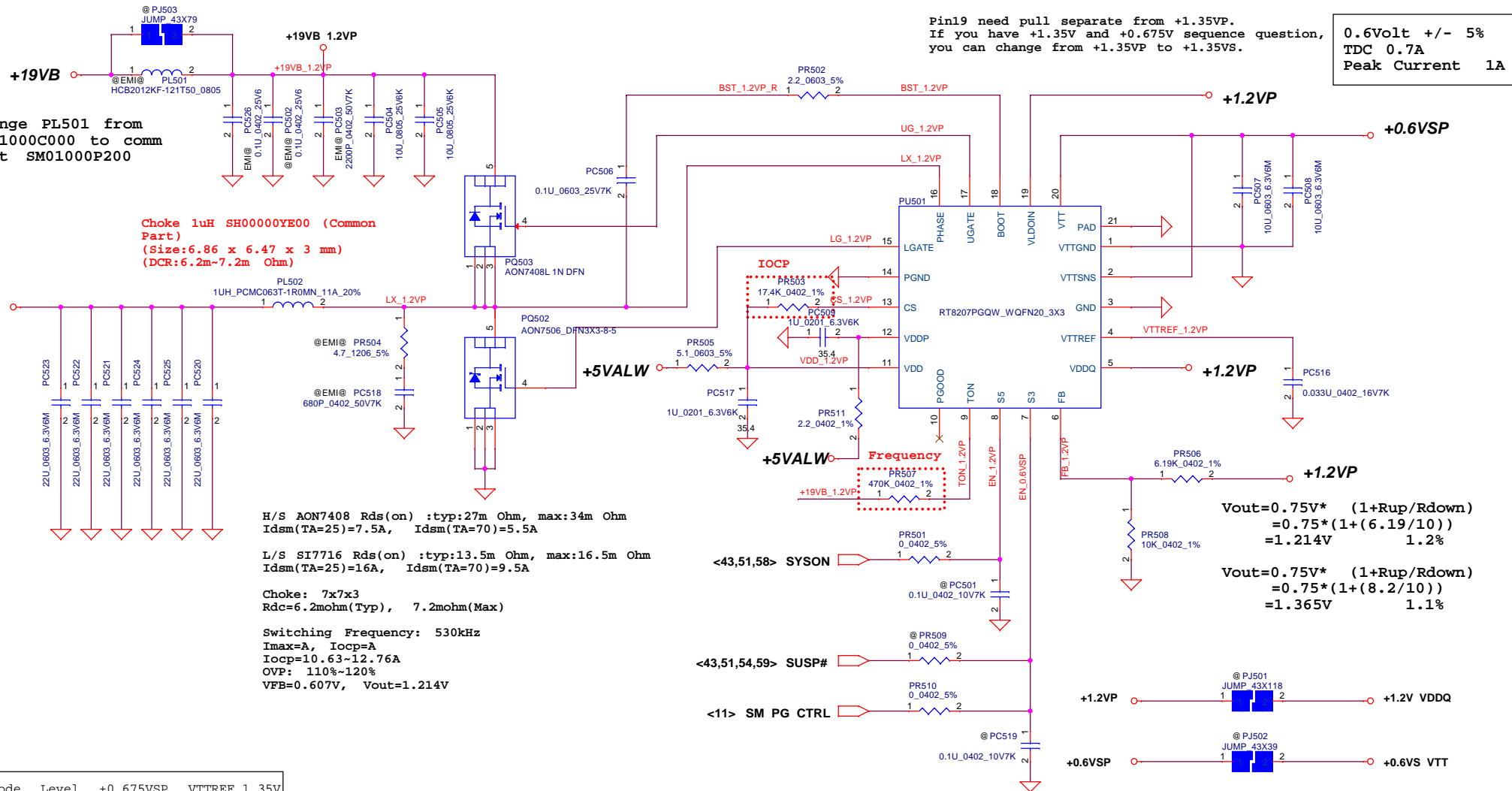
Vout is 3.234V~3.366V
Ipeak=4.65A
Imax=3.25A
Iocp=10A

Choke 1.5uH SH000016700 (Common Part)
(Size:7.3 x 6.6 x 3 mm)
(DCR:14m-15m)

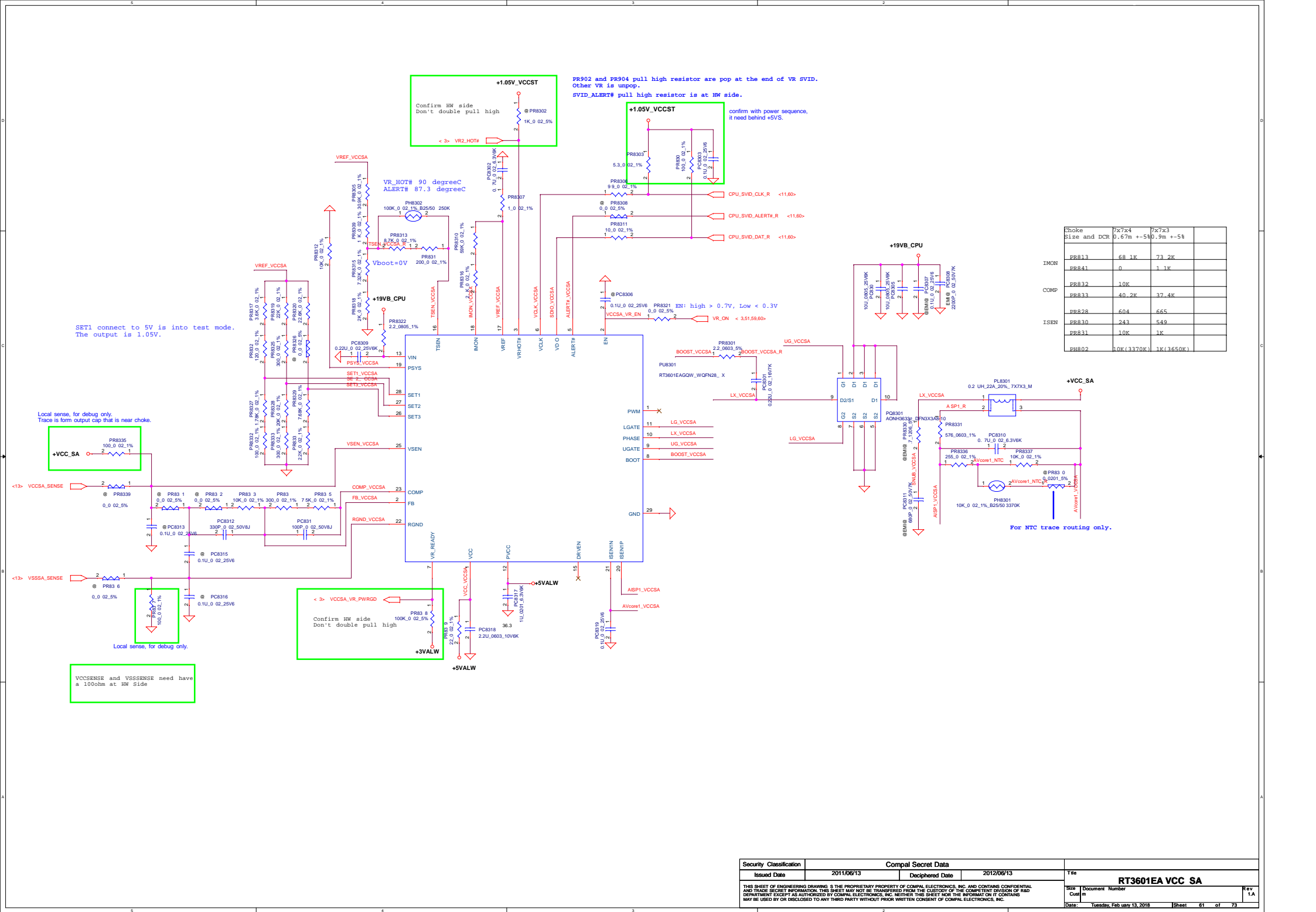
Vout is 4.998V~5.202V
Ipeak=9A
Imax=6.6A
Iocp=10A



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Issued Date	2016/11/03	Deciphered Date	2017/06/14	3.3VALWP/5VALWP	
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SET1 connect to 5V is into test mode.
The output is 1.05V.

Local sense, for debug only.
Trace is form output cap that is near choke.

VCCSENSE and VSSSENSE need have
a 100ohm at HW Side

+1.05V_VCCST
Confirm HW side
Don't double pull high
< 3> VR2_HOT#

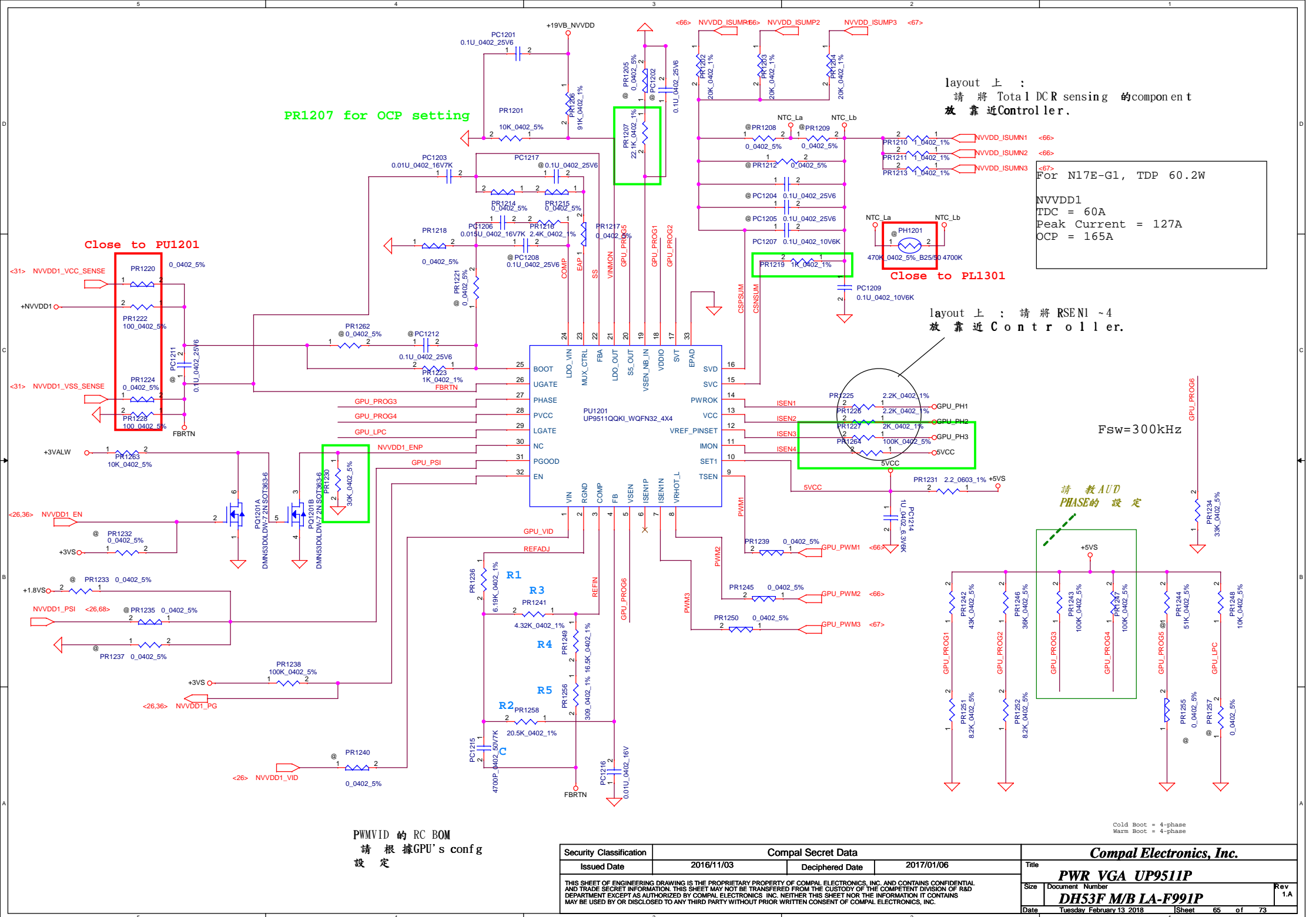
PR902 and PR904 pull high resistor are pop at the end of VR SVID.
Other VR is unpop.
SVID_ALERT# pull high resistor is at HW side.

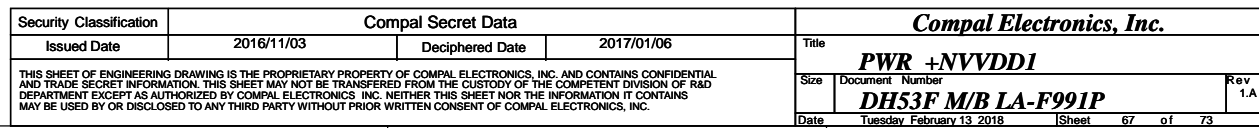
+1.05V_VCCST
confirm with power sequence,
it need behind +5VS.

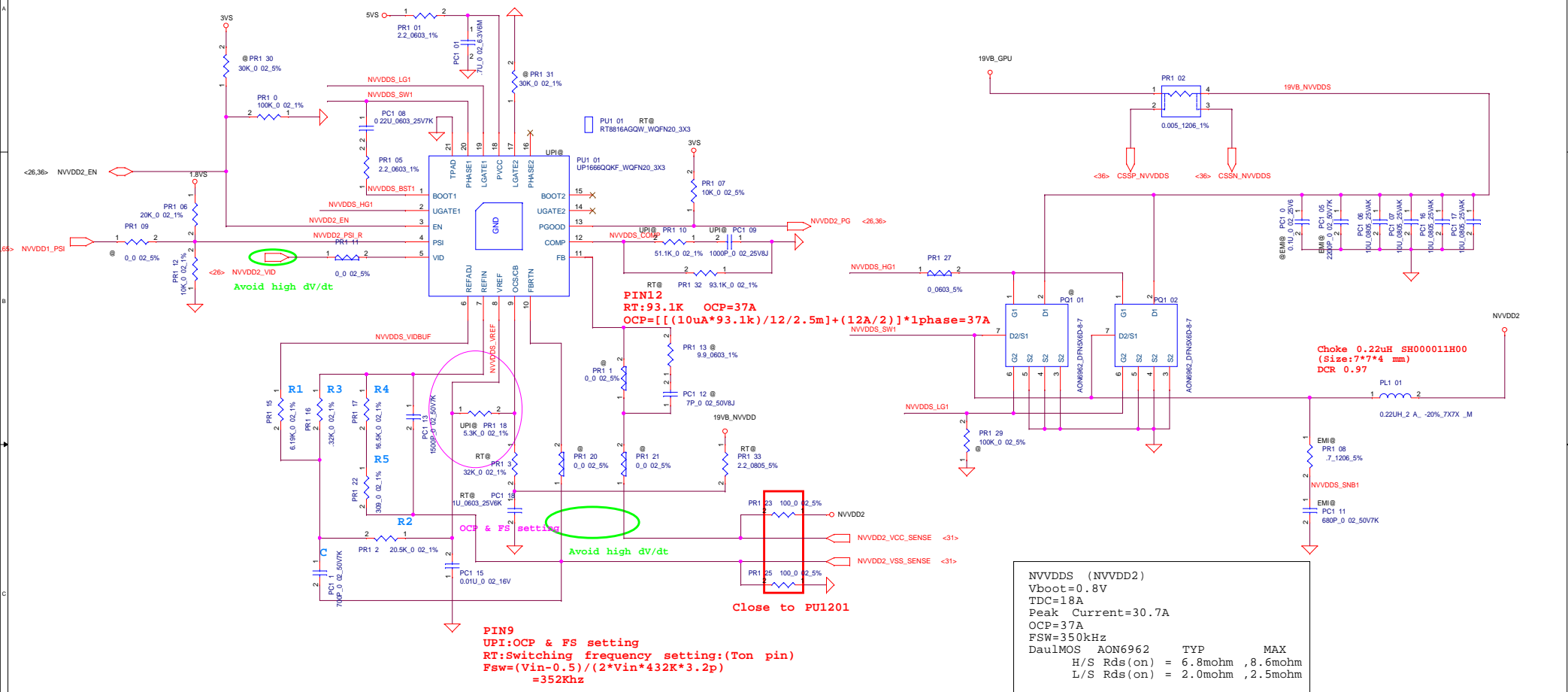
+3VALW
Confirm HW side
Don't double pull high

Choke	Size and DCR	7x7x4	7x7x3
PR813	68 1K	73 2K	
PR841	0	1 1K	
PR832	10K		
PR833	40 2K	37 4K	
PR828	604	665	
PR830	243	549	
PR831	10K	1K	
PR802	10K(13370K)	1K(13650K)	

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2011/06/13	Deciphered Date	2012/06/13
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		Down Size	0.1		PQ311,PQ312: AON6366E 1N DFN5X6-8SB00001D800->AON7380_DFN3X3-8-5SB000016M00 PC302,PC303,PC310,PC311,PC312: 10U_0603_25V6MSE00000X200->10U_0805_25V6KSE00000QK00 PC323: 10U_0603_25V6MSE00000X200->Del PC315,PC1312,PC1324,PC1362,PC1411: 680P_0603_50V7KSE025681K80->680P_0402_50V7KSE074681K80/26 PC412,PC426,PC602,PC7203,PC8311: 680P_0603_50V7KSE025681K80->680P_0402_50V7KSE074681K80Unpop PC102: 100P 50V J NPO 0603SE024101J80->100P 50V J NPO 0402SE071101J80 PC104: 1000P 50V K X7R 0603SE025102K80->1000P 50V K X7R 0402SE074102K80 PQ1401: AON6962_DFN5X6D-8-7SB00001ID00->Unpop		
02		Down Size & NVVDDS IC COLAY	0.1		PR1301,PR1302,PR1402: 0.005_2512_1%SD000016U00->0.005_1206_1%SD000017R00 PC1410: 0.1U_0603_16VSE026104K80->Del PR1432: Add->93.1K_0402_1%SD034931280 PR1410: 51.1K_0402_1%SD034511280->un pop PC1409: 1000P_0402_25V8JSE068102J80->un pop PU1401: UP1666QKQF_WQFN20_3X3SA000095X00->RT8816A6QW_WQFN20_3X3SA00009WE00 PR1414: 10K_0402_5%SD028100280->0_0402_5%SD028000080 PR1418: 45.3K_0402_1%SD034453280->un pop PR1419: 84.5K_0402_1%SD034845280->Del PR1433: Add->2.2_0805_5%SD002220B80 PC1418: Add->1U_0603_25V6KSE000006900 PR1434: Add->432K_0402_1%SD034432380 PC8134: 0.1U_0402_50V7KSE074104K80->0.1U_0402_25V6SE000006880	10/26	A
03		CPU TEST	0.1		PU501_RT8207PGQW_WQFN20_3X3 -> RT8207PGQW_WQFN20_3X3-S PH8103,PH8104_150K_0402_5%_B25/50_4500K_SL200002K00 -> S THERM 220K +-5% 0402 B25/50 4700K_SL200002I00 PR8110, PR8109_8.87K_0402_1%_SD034887180 -> 8.66K_0402_1%_SD034866180 PR8118, PR8119_93.1K_0402_1%_SD034931280 -> 57.6K_0402_1%_SD034576280 PC8113,PC8124,PC8140,PC8159,PC8163_0.47U_0402_16V4Z_SE000002F80 -> 0.47U_0402_6.3V6K_SE124474K80 PC8310_0.47U_0402_25V6K_SE00000WA00 -> 0.47U_0402_6.3V6K_SE124474K80 PR8114_6.81K_0402_1%_SD034681180 -> 5.76K_0402_1%_SD034576180 PR8113_2.49K_0402_1%_SD034249180 -> 1.8K_0402_1%_SD00000R580 PR8117_560K_0402_1%_SD034560380 -> 442K_0402_1%_SD034442300 PR8116_510K_0402_1%_SD00000RK80 -> 402K_0402_1%_SD034402380 PR8141_100_0402_1%_SD034100080 -> 8.2K_0402_1%_SD000004100 PR8149_1.05K_0402_1%_SD00000J480 -> 3.16K_0402_1%_SD000006580 PR8176_20K_0402_1%_SD034200280 -> 16.9K_0402_1%_SD034169280 PR8310_63.4K_0402_1%_SD03463K280 -> 59K_0402_1%_SD034590280 PR8319_24.9K_0402_1%_SD034249280 -> 22K_0402_1%_SD034220280 PR8325_0_0402_5%_SD028000080 -> 300_0402_1%_SD034300080 PR8328_22K_0402_1%_SD034220280 -> 20K_0402_1%_SD034200280 PR8333_680_0402_1%_SD034680080 -> 300_0402_1%_SD034300080 PC8312_270P_0402_50V7K_SE074271K80 -> 330P_0402_50V8J_SE000006I80 PR8331_470_0603_1%_SD014470080 -> 576_0603_1%_SD014576080 PR8336_42.2_0402_1%_SD00000ZNO0 -> 255_0402_1%_SD034255080 PC9110 PC9108_22U_0603_6.3V6M_SE00000M000 -> unpop PC9112 PC9113_unpop -> 22U_0603_6.3V6M_SE00000M000 PC8126,PC8137_330P_0402_25V8J_SE00000F80 -> 330P_0402_50V8J_SE000006I80 PR8134_121K_0402_1%_SD034121380 -> 13.3K_0402_1%_SD034133280 PR8138_49.9K_0402_1%_SD034499280 -> 26.7K_0402_1%_SD034267280 PR8147_3.32K_0402_1%_SD034332180 -> 768_0402_1%_SD00000TT80 PR8173_0_0603_5%_SD013000080 -> 10_0603_1%_SD014100A80	10/26	A
04		down size &CHANGE VGA IC	0.2		PU1201_UP9511PQGJ_VQFN40_5X5_SA00009SW00 -> UPI9511QQKI_WQFN 32P_SA0000BK300 PC8317,PC509,PC517_1U_0402_10V6K_SE00000QL10 -> 1U_6.3V_K_X5R_0201_SE00000YB00 PC8112,PC8115,PC8123,PC8139,PC8157,PC8161_1U_0402_25V6K_SE000010V00 -> 1U_6.3V_K_X5R_0201_SE00000YB00 PQ307_LMUN5113T16_PNP_SOT323-3_SB000013X00 -> Unpop PQ308_LMUN5236T16_NPN_SOT323-3_SB000011K00 -> Unpop PQ313_2N7002KDW_2N_SOT-363-6_SB00000EO00 -> Unpop PQ314_RUM001L02_1N_VMT3_SB000012900 -> Unpop PR340_10K_0402_1%_SD034100280 -> Unpop PR327_0_0603_5%_SD013000080 -> Unpop PR326_0_0603_5%_SD013000080 -> SMT PR310_51.1K_0402_1%_SD034511280 -> 52.3K_0402_1%_SD034523280 PC1709_220U_D2_5X_2VY_R9M_SGA0000BT00 -> Unpop PC8147_10U_0805_25V6K_SE00000QK00 -> Unpop	11/08	A
05		Unpop reduce charger IC loss extra circuit. Unpop GPIO12& PROCHOT synchronous circuit.	0.2			11/15	A

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Item	Fixed Issue	Rev.	PG#	Modify List	Date	Phase
01	Oohm ->R-Short	1.0		PR326,PR304,PR314,PR316,PR317,PR322,PR333,PR334,PR8111,PR8120,PR8128,PR8129,PR8139,PR8142,PR8143,PR8153,PR8154,PR8155,PR8163,PR8165,PR8170,PR8175,PR8184,PR8190,PR8198,PR8204,PR8308,PR8339,PR8341,PR8342,PR8346,PR8326,PR1414_SD028000080 chage to _R-Short 0402 PR326 0_0603_5%_SD013000080 ->R-Short 0603_SD013000080	12/17	A.2
02	material shortage	1.0		PC313,PC314_1U_0402_16V6K_SE000000U00_->_1U_6.3V_K_X5R_0201_SE000000YB00 PC1303,PC1314,PC1353,PC8101,PC8122,PC8135,PC8150,PC8158 _0.1U_0603_50V7K_SE025104K80_->_0.1U_25V_K_X7R_0603_SE042104K80 PC305,PC324_0.1U_0402_25V7K_SE000000W210_->_0.1U_0402_25V6_SE000000G880	12/17	A.2
	Acer SW2 design reserve	1.0		PR217 0_0402_5%_SD028000080(unpop) -> SMT 0402_SD028000080	12/17	A.2
03	For 4S per cell 4.35V battery	1.0		PQ307_LMUN5113T1G_SOT323-3_SB000013X00_->del PR327unpop_0_0603_5%_SD013000080_->del PR342Add_->_2M_0402_1%_SD034200480 PR343Add_100K_0402_1%_SD034100380 PQ315Add_2N7002KW_SOT323-3_SB000000ST00	12/20	A.2
04	charger boost cap to 0.47uF but material shortage so down size.	1.0		PC309_0.22U_0603_25V7K_SE0000005Z80_->_0.47U_0402_16V4Z_SE0000002F80	12/21	A.2
05	ACDET change	1.0		PR306_392K_0402_1%_SD034392380_->_499K_0402_1%_SD034499380 PR310_52.3K_0402_1%_SD034523280_->_66.5K_0402_1%_SD034665280	12/28	A.2

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	46	USB	10/18	Correct USB charger connection.	1.Change RS15 connection to CHG_ILMSEL.	DVT	0.2
2	19,36	Placement	10/18	Placement	1.Remove RPH10, add RH197,RH198. 2.UG27 source change to +1.8VALW for +1.8VSDGPU_AON/+1.8VSDGPU_MAIN.	DVT	0.2
3	41	CNVI	10/18	For CNVI power rail.	1.Co-lay RM46 for CNVI +3VALW power rail.	DVT	0.2
4	42	Material	10/18	X1 code issue.	1.LA1 change to SM01000NS00.	DVT	0.2
5	48	USB	10/18	redriver verify.	1.Add one USB3.0 port to JIO3.	DVT	0.2
6		Placement	10/21	Placement	1. Change RM36,RM37,RM42,RM43 to 0402 size. 2. Change RH186,RH47,RH98~RH100,RH103,RH105,RD2,RD3,RD6,RD13,RD15,RD17,RM34,RM35,RM38,RM39,RS1,R19,R20,RQ5,RQ6,RQ9 to R-short. 3. Change RS8,RS10 to 1206 R-short. 4. Change RH97 to 0805 R-short.	DVT	0.2
7	11	ESD cap.	10/21	Sourcer request.	1.Change CC66,CC68 to SE074102K80.	DVT	0.2
8	43	EC	10/21	EC board ID.	1.Change RB3 to 12kohm/28P@ and 160kohm/32P@	DVT	0.2
9		Cap.	10/24	Sourcer request.	1. Change CA6,CA8,CA9,CA12,CA14,CA16,CA19,CC71~CC81,CC88~CC90,CG130,CG131,CG143~CG145,CG168,CG169,CG178~CG181,CG193,CG205~CG207,CG229,CG230,CG241,CG243,CG253~CG255,CG267~CG269,CG291,CG292,CG303~CG305,CX1,CX3 from 0402 to 0603 size.	DVT	0.2
10	50	Screw hole	10/25	Screw hole	1.Change H21 footprint to H_6P0.	DVT	0.2
11	48	USB EMI	10/25	EMI issue.	1.Add LS11,LS12.	DVT	0.2
12	41,43	CNVI	10/26	For CNVI power rail detect.	1.Add net CNVI_DET#,RB78,RB79.	DVT	0.2
13	46	USB	10/26	Correct USB charger connection.	1.Correct USB2.0 connection for US12.	DVT	0.2
14	42	DMIC	10/26	Acer request.	1.Change JDMIC1 from 8pin to 4pin.	DVT	0.2
15	47	SATA	11/03	Co-layout.	1.Co-lay JHDD3,CO14~CO17,RO21~EO24.	DVT	0.2
16	44	SMBus	11/08	Co-layout.	1.Co-lay RS114,RS115.	DVT	0.2
17	49	SW	11/14	Remove debug SW.	1.De-pop SW1.	DVT	0.2
18	44	Type-C	11/14	CC logic control by EC SMBus.	1.De-pop QS1,QS3,RS107,RS108,RS111. Pop RS114,RS115.	DVT	0.2
19	16	Cap.	11/14	by crystal vendor test result.	1.Change CH7,CH8 to 10pF.	DVT	0.2
20	45	Cap.	11/16	For shortage.	1.Change CS84~CS87 to SE00000G880.	DVT	0.2
21	43	CNVI	11/16	CNVI detect by SW.	1.De-pop RB78. Pop RB79.	DVT	0.2
22	43	CNVI	12/15	Remove CNVI detect.	1.Remove RB78, RB79 and netname CNVI_DET#.	PVT	1.0
23	18	PECI	12/15	For Peci issue.	1.De-pop RH41.	PVT	1.0
24	50	BI SW	12/15	By customer request.	1.De-pop SW2.	PVT	1.0
25	43	EC	12/15	Update EC board ID.	1.Change RB3 to 15kohm/28P@ and 200kohm/32P@	PVT	1.0
26	42	Inductor	12/15	Change source.	1.Change LA1 to SM01000EE00.	PVT	1.0
27		NPI	12/15	For NPI test.	1.Change RB19,RC17,RG143,RG200,RG202,RH101,RH102,RH5,RH6,RH92,RH93,RH94,RH96,RM2,RS114,RS115,RB72,RB76,RL1,RL13,RQ2 to R-short.	PVT	1.0

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28	44	Type-C	12/18	Change current limit solution	1.Change US2 to SA00006Y700. 2.Add RS116,RS117,RS118. Reserve CS101.	PVT	1.0
29	43	EC	12/20	For PWR BATT_4S	1.Add net BATT_4S to EC pin89.	PVT	1.0
30	41	WLAN	12/20	For CNVi BT_ON	1.Add RM47.	PVT	1.0
31	21	PCH	12/20	For intel sensitive net	1.Pop CH29,CH34,CS100.	PVT	1.0
32	45	Type-C	12/21	For intel new topology	1.Change RS64,RS65,RS74,RS76,RS82~RS85 to 0201 size. 2.Add CS102~CS105,RS119~RS122.	PVT	1.0
33	36	GPU	12/21	Fine tune GPU sequence	1.Change CG315 to 0.22uF, RG190 to 16.9k ohm, add RG225.	PVT	1.0
34	20		12/28	For MB ID	1.De-pop RH86. Pop RH85,RH87.	PVT	1.0
35	7,15	CPU,PCH	12/28	Update intel chip to QS PN	1.SA0000BPJ10 for i5@, SA0000BPI10 for i7@, SA0000BPF10 for PCH@.	PVT	1.0
36	7	DAZ	12/28	Update MB DAZ PN.	1.DAZ29000100 for PCB@.	PVT	1.0
37	37	eDP	12/28	For eDP sequence	1.Pop RX1.	PVT	1.0
38	18,39	PCIE	01/11	For IRST support issue.	1.Change PCIE port17~20 to port 9~12 for PCIE SSD. 2.Change SATA port0A to port4 for SATA HDD. 3.Change SSD_DEVSLP4 to SSD_DEVSLP1. 4.Change SATA_GP4 to SATA_GPI.	PVT	1.C
39	45	Type-C	01/11	For intel new topology	1.Place CS58~CS61 close to connector and change net name.	PVT	1.C
40	43	EC	01/11	Update EC board ID.	1.Change RB3 to 20kohm/28P@ and 240kohm/32P@	PVT	1.C
41	21	PCH	01/12	For layout routing.	1.Change RH93 to 0ohm footprint.	PVT	1.C
42	45	Type-C	01/16	For intel new topology	1.Change CS58~CS61 to 0.22uF.	PVT	1.C
43	7	CPU,DAZ	01/27	Update CPU,DAZ PN	1.SA0000BPZ10 for i7@, DAZ29000103 for PCB@.	PVT	1.C
44	7,15	CPU,PCH	02/13	Update CPU,PCH PN to MP PN.	1.SA0000BPJ40 for i5@,SA0000BPZ40 for i7@,SA0000BVP10 for PCH@.	Pre-MP	1.C

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